Bulk FinFET Device Characteristics and Integration Process with All-Last HKMG

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Abstract

Device characteristics and integration scheme of bulk FinFETs with All-Last HKMG process, as shown in Figs. 1 and 2, are investigated. The issues that bulk FinFET integration has are discussed and the solutions and/or possible solutions are presented. Both nFinFETs and pFinFETs were built with EOT=9A and the minimum gate length of 20nm patterned by e-beam lithography. For pFinFET@Lg=25nm, the Vt_sat, DIBL and sub-threshold swing (SS) are -0.245V, 69mV/V and 68mV/dec, respectively. For nFinFET@Lg=25nm, the Vt_sat, DIBL and SS are 0.351V, 76mV/V and 83mV/dec. All measurements were conducted under Vdd = 0.8V. Spacer-transfer-layer-patterning technology was used to form fins. A novel planarization technique, Advanced Physical Planarization (APP), is introduced for the first time to replace CMP and obtain good control of fin and dummy gate height. Wafer-to-Wafer variation of APP is less than 2nm and much smaller than that of CMP, which is crucial for bulk FinFET integration. Punch through stopper layers under fins are formed by specially designed ion implantations. Gap filling capability of Vt tuning metals and its effects on device characteristics were investigated. By developing multi-step plasma RIE method and adjusting over etch parameters, the etching damages on fin top surfaces during dummy gate and spacer formation are reduced and well controlled. Therefore, good profiles of the dummy gate and spacers are obtained.

Bulk FinFET integration scheme developed in this paper is designed for potential industry application and balanced between solving main technical issues and the compatibility of standard industry processes.

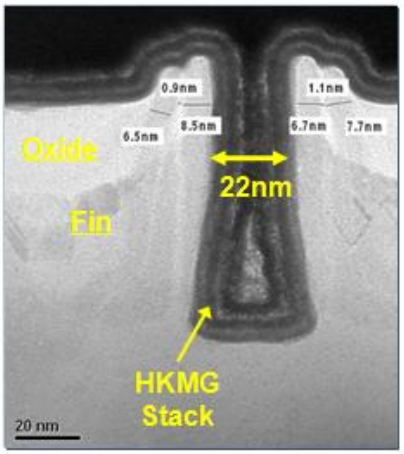

Fig. 1 TEM crossing HKMG on the fin of a pFinFET.

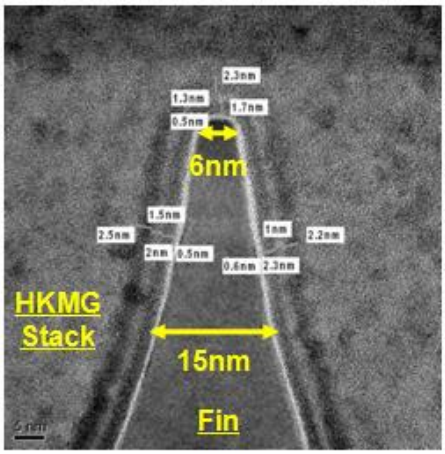

Fig. 2 TEM crossing fin in the HKMG of a pFinFET.