Invited Paper

Electrostatic Discharge Protection of Nano-Scale SOI CMOS

Dimitris E. Ioannou
ECE Department, George Mason University, Fairfax, VA 22030
Email: dioannou@gmu.edu; Tel: (703) 9931580

SOI chips face unique challenges with regard to ESD protection due to the geometrical nature of the structure itself: the silicon film is separated from the substrate by the buried oxide layer, which has much lower thermal conductivity than silicon. The active layers are thus both electrically and thermally separated from the substrate, rendering conventional ESD protection circuits such as thick field oxide devices and vertical, large area p-n diodes, unsuitable because of the absence of vertical current and heat flow paths. Consequently, it was recognised quite early in the development of SOI technologies that there was a need to form ESD current and heat flow paths above the active layers; or some other clever solutions must be found that can make use of the substrate for building the ESD protection circuitry underneath the buried oxide. The situation has gotten worse with each successive SOI CMOS generation, because of the continuously shrinking SOI silicon film thickness. In the search for a solution to this problem, several new approaches have been taken; for example, structures using vertical current paths have been developed by opening holes through the buried oxide in selected locations through which the ESD current is "pushed" to the ground.

At the moment, and for the foreseeable future, the "hottest" SOI CMOS technologies are based on "ultra thin" body fully depleted (FD) SOI MOSFETs and FinFETs, where the very limited amount of silicon present in the channel makes a bad ESD situation worse. However, relentless research has developed sufficiently robust ESD protection designs, such that this problem is no longer considered to be a "show stopper". In this talk, after briefly recognizing the special requirements for the ESD protection of SOI chips, we will review the state of the art of the most promising designs for ESD protection of FD and FinFET SOI nano-CMOS technologies, and will attempt to make some projections for the foreseeable future, as we approach the "end" of the International Technology Roadmap for Semiconductors (ITRS).