Invited

Analog and Digital Switching Characteristics of Transition Metal Oxide Based Resistive Random Access Memory (ReRAM) Devices

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Transition Metal Oxide (TMO) Based Resistive Random Access Memory (ReRAM) devices have gathered significant research attention for non-volatile data storage applications. The major advantages lie in terms of scalability, low switching voltages, and process compatibility with the CMOS technologies [1, 2]. However, to take the complete benefit of this enabling technology there are several challenges that need to be addressed. This talk will present our work towards addressing these challenges for ReRAM devices.

It is well known that a one-time electroforming is typically needed to activate the growth of filament in TMO and initiate the switching process [3]. The process of electroforming can have significant impacts on the device switching characteristics, endurance, variability, and reliability which is not well-understood. This talk will discuss the cause of switching failure associated with the electroforming and present a novel technique of forming the devices. Data will be presented to compare the endurance, yield, and repeatability of the device performance with various forming processes. The role of certain dopants in TMO towards an effort for reducing the forming voltages will be discussed. Thereafter, the presentation will focus on understanding the mechanism of switching in ReRAM devices. Though the prevalent theory of "filament formation and re-oxidation" has been widely accepted now, the chemical kinetics of filament re-oxidation during the reset process has not been supported by sufficient experimental evidences [4]. As a result, the existing device models are insufficient in capturing the kinetics of reset in ReRAM devices. To elucidate the reset process in ReRAM devices, we will discuss our work on temperature based reset studies in ReRAM devices that can provide useful information about the re-oxidation or retraction process of filaments in TMO during the reset process of the devices.

This talk will also discuss the characteristics of multi-level-cell (MLC) in ReRAM devices that can provide low-cost/Gigabyte storage solutions. The read/write/erase energies for various states will be discussed that can have significant impact on various computer architectures [5]. The role of sneak current in high-density crossbar architectures of ReRAM devices and the targeted specifications of diode towards minimizing the sneak current in 1 diode 1 ReRAM (1D 1R) architecture will be discussed [6].

Finally, we will discuss our results on analog ReRAM devices in which the conductance of the device can be reconfigured continuously as a function of the applied voltage pulse. Such devices will be referred as *Synaptic Memory* devices. The cause of an analog change in the conductance will be discussed and applications in the areas of Neuromorphic computing will be presented [7].

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