Student Paper

Scaling Issues and Solutions for Double Gate MOSFETs at the end of ITRS

Mehdi Salmani-Jelodar, SungGeun Kim, Kwok Ng*, Gerhard Klimeck
Network for Computational Nanotechnology, Purdue University, West Lafayette, IN-47906, USA.
*Semiconductor Research Corporation, Research Triangle Park, North Carolina, USA.
*Tel: (+1)765-237-8828, Email: m.salmani@gmail.com

Introduction: MOSFET device size shrinking leads to significant performance degradations due to short channel effects (SCEs) in bulk device geometries. Today's double-gate (DG) structures mitigate and reduce these SCEs. Further down-scaling below the 10 nm gate lengths encounters another detrimental device performance reduction: source-to-drain (S/D) tunneling [1]. In this work, the possibility of scaling DG MOSFETs as depicted in Fig. 1 is investigated at the end of ITRS roadmap [2] by answering two questions: 1) How much does S/D tunneling impact device performance? 2) What are the possible solutions?

As it is shown in Fig. 2, tunneling probability depends on three factors: i) The barrier height (H) which is controlled by the gate voltage, ii) Carrier effective mass (m*) which depends on the material and device geometry and iii) The barrier length (X) which heavily relies on the L_{Eff}. S/D tunneling effect can be suppressed using different methods, such as heavier mass carriers or through/by optimizing source/drain doping profile [2]. This work analyzes the impact of S/D tunneling by measuring the tunneling current ratio (TR) over the whole leakage current in the OFF-state. To show the impact of tunneling on overall device performance, the channel length is varied while other device parameters are kept constant. Using heavier carrier effective mass and optimizing doping profile are some possible approach to reduce TR. Carrier effective mass optimization with changing channel transport and confinement orientations is shown to be able to boost the device performance.

Methodology: The initial device specifications are the same as the ITRS table for 2028. The effective channel length (L_{eff}) is determined as 80% of the gate length in the ITRS table and the body thickness (t_{si}) as 40% of the L_{Eff} (Fig. 1) [2]. The modeling is carried out by the state-of-the-art quantum transport simulator with the $sp^3d^5s^*$ tight binding [4]. The total achieved current is divided by 2 to report the current per width each side. The OFF-current is set to 100 nA/μm. The energy resolved current reveals the distinction of tunneling and over-the-barrier transport (Fig. 2).

Results and discussion: A double-gate device as depicted in Fig.1 is modeled. The ballistic characteristics of the device with L_{Eff}=4.1 nm and Si <100>/[100] (from ITRS tables [2]) is calculated. To identify the effects of tunneling, the same device with longer channel, e.g. L_{Eff}=6.1 nm, is simulated and the I_D-V_G is depicted in Fig. 3 which shows a huge improvement in longer channel device. TR, as reported in Table I, reduced from 98% to 79% which has a dramatic effect on sub-threshold swing (SS) and improves from 98 to 77 mV/dec. This improvement in SS leads to a better V_{th} and consequently ~57% improvement in ON-current. At L_{Eff}=4.1 nm the OFF-current is composed of mostly the tunneling current (Fig. 4), but in the case of 6.1 nm it is a combination of the thermionic and the tunneling current (Fig. 5).

As the drawback of S/D tunneling is evident, we can find solution which keeps the channel length fixed but improves the device performance using a heavier carrier effective mass. Silicon with different orientation provides different transport mass [5]. Band structure and respectively, the carrier effective mass change with rotating the transport/confinement orientation from <100>/[100] to <111>/[110] or <111>/[11-2] (see Table I). Both cases improve the SS value (94 and 89 mV/dec respectively) but they behave differently for ON-current (2200 and 1370 uA/um respectively). Although, Si<111>/[11-2] provides heavier mass and reduces the tunneling ratio from 98% to 69% (Fig. 6) and improves the SS, from 98 to 89 mV/dec, it cannot provide good ON-current. This is due to very low injection velocity. However, Si<111>/[110] provides better SS and ON-current than Si <100>/<100> (Fig. 7). This indicates that there is a trade-off between SS and ON-current and an optimum mass is required to keep the ON-current high.

Conclusions: S/D tunneling degrades the device performance drastically. Engineering the carrier effective mass through crystal orientations, confinement and strain can provide a means to design a carrier effective mass for better device performance. **An optimum mass needs to be heavy enough to reduce tunneling current while light enough to keep the injection velocity high to provide high ON-current.** Potential design examples are shown. An optimized DG device show that for L_{Eff}=4.1 nm, the transport direction <111> with confinement [110]

gives the best performance among the tested three orientations. However, further study is required for other solutions, such as doping profile optimization and strain engineering.

References: [1] M. Salmani-Jelodar, et al., "Rewriting the ITRS Device Tables," in prep. to submit to Applied Physics Letters, 2013, [2] ITRS 2013, available online http://www.itrs.net/ [3] S. Mehrotra, et al., "Engineering Nanowire n-MOSFETs at Lg < 8nm," IEEE TED, vol. 60, no. 7, pp. 2171-2177, 2013 [4] M. Luisier et al, "Atomistic simulation of nanowires in the sp3d5s* tight-binding formalism: From boundary conditions to strain calculations," Phys. Rev. B ,vol. 74, no. 20, p. 205323, 2006. [6] N. Neophytou, A. Paul, M.S. Lundstrom, G. Klimeck, "Bandstructure effects in silicon nanowire electron transport ," Trans. Elec. Dev., 55, 1286

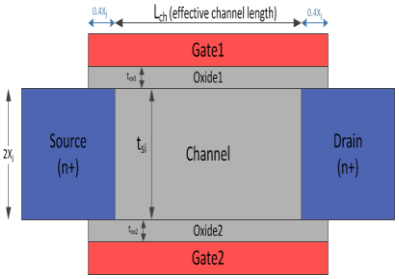

Fig 1. Schematic of the DG device. From the ITRS table, Lg = 5.1 nm and L_{Eff} is 4.1 nm. The EOT = 0.41 nm. Si is the channel material and V_{DD}=0.64 V.

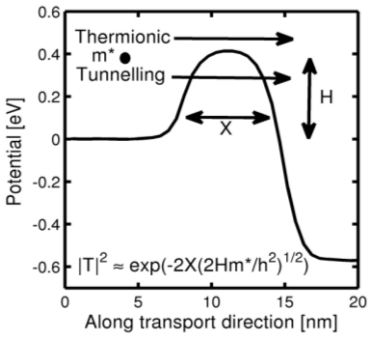

Fig 2. S/D tunneling probability dependence on barrier height (H), carrier effective mass (m*) and barrier length (X).

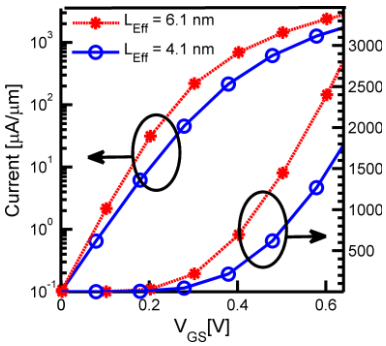

Fig 3. Id-Vg characteristics for DG with Si <100>/[100] channel and different L_{Eff} (4.1 and 6.1 nm). Longer channel device outperforms with 57% higher ON-current.

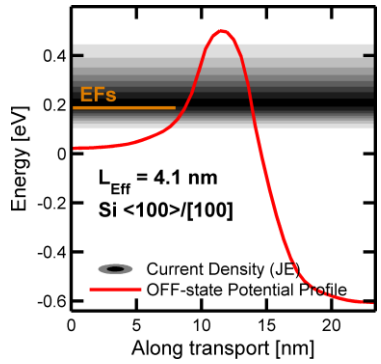

Fig 4. The current spectrum mainly composed of the tunneling current (98%) at L_{Eff} = 4. 1 nm (at k_y=0).

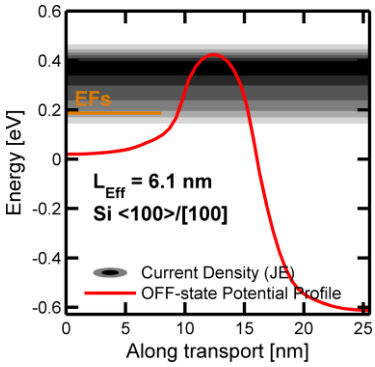

Fig 5. The current spectrum partially composed of the tunneling current (79%) at L_{Eff} = 6.1 nm (at k_y=0).

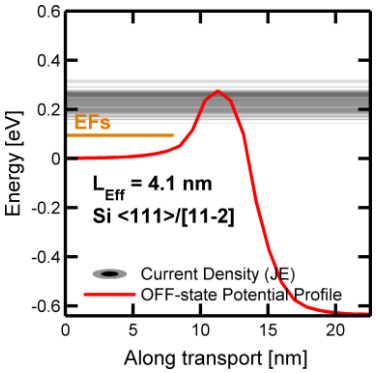

Fig 6. The current spectrum partially composed of the tunneling current (69%) with Si <111>/[11-2] (at k_y=0).

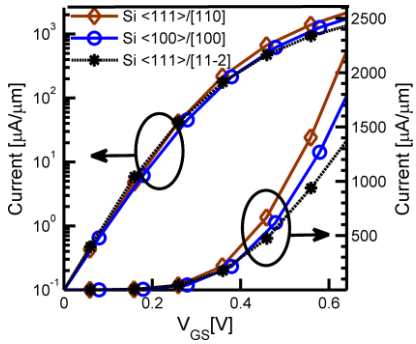

Fig 7. I_D-V_G characteristics for different transport orientations in logarithmic (left axis) and linear (right axis) plot where shows Si<111>/[110] outperforms.

	m^*/m_0	TR [%]	SS [mV/dec]	ION [uA/um]
<100>/[100], L_{EFF}=4.1 nm	0.2	98	98	1790
<100>/[11-2], L_{EFF} =4.1 nm	0.476	69	89	1370
<111>/[110], L_{EFF} =4.1 nm	0.22	98	94	2200
<100>/[100], L_{EFF} =6.1 nm	0.2	79	77	2810

Table I. Electron effective mass at the bottom of conduction band (m*), tunneling ratio (TR), SS and ION for all four cases are shown. At the same L_{Eff} (e.g. 4.1 nm) Si<111>/[110] gives the highest ION.