Scalable 3D III-V Nanowire Electronics by MOCVD

Xiuling Li[1,*], Xin Miao[1], Chen Zhang[1], Kelson D. Chabak[1,2], Ryan Dowdy[1], Parsian Mohseni[1], Kyooho Jung[1], Wonsik Choi[1], and Dennis E. Walker Jr.[2]

[1] *Department of Electrical and Computer Engineering, Micro and Nanotechnology Laboratory, University of Illinois at Urbana-Champaign, 208 N. Wright St., Urbana, Illinois, 61801*
[2] *Sensors Directorate, Air Force Research Laboratory, 2241 Avionics Circle, Wright-Patterson Air Force Base, OH 45433 USA*
** e-mail: xiuling@illinois.edu*

Planar nanowires (NWs) grown by metalorganic chemical vapor deposition (MOCVD) represent a new nanowire paradigm that is site-controlled, self-aligned, defect-free, transfer-printable, and compatible with planar processing technologies. This talk will focus on our recent results on using this platform technology for high speed low power nanoelectronics. In particular, the selective lateral epitaxy nature of the Au-assisted vapor-liquid-solid (VLS) growth of III-V semiconductors, crystal orientation dependent alignment, lateral p-n junctions and heterojunction formation, DC and RF performance of HEMTs, MESFETs, and MOSFETs fabricated using the planar nanowire array as the channel material, will be discussed [1-7]. Because of the inherent 3D cross-section of these NWs, this is essentially a 3D III-V platform for high frequency low power electronics.

Fig. 1 shows the development roadmap of this platform that involves complete site control to yield unidirectional alignment (Fig. 1a), formation of lateral p-n junction in situ monolithically (Fig. 1b), lateral heterojunction formation (Fig. 1c), and ultimately array-based nanowire transistors with desired density, dimension, and junctions on arbitrary substrates (Fig. 1d). Fig. 2 shows an array of self-aligned planar GaAs nanowires grown using MOCVD via the Au-assisted VLS mechanism on a GaAs (100) substrate. The Au nanoparticles were patterned on the GaAs substrate using electron beam lithography (EBL) before the substrate was loaded into the growth chamber. It is critical to ensure the cleanness of the substrate surface as well as the purity of the MOCVD precursors in order to maximize the planar nanowire yield. (110) substrates, where only one <111>B direction is available, are required in order to achieve unidirectional alignment because the planar nanowires are projections of <111>B. In addition to planar GaAs nanowires, planar InAs nanowire and InAs/GaAs heterojunction growth and doping will also be reported.

We have demonstrated a simple amplifier as shown in Fig. 3, with a single-NW MESFET used as the active device and the other single-NW device as the current-source load. The maximum voltage gain we obtained is ~120. The extracted channel length modulation parameter λ is 0.02 V^{-1}, which is lower than the typical value of 0.1~0.3 V^{-1} for conventional GaAs MESFETs. We believe this improvement can be attributed to the multi-gate geometry of the planar NWs. In addition to MESFETs, we have successfully demonstrated depletion-mode MOSFETs using the planar trapezoidal shaped GaAs NWs with ALD Al_2O_3 as the gate oxide. Figure 4 shows the effect of an interlayer between the high-k gate oxide Al_2O_3 and n-GaAs surface on the DC performance of the NW MOSFETs. For the device without a silicon oxide interlayer, the transconductance is lower and it quickly rolls off after the gate voltage reaches ~1 V beyond threshold. In contrast, the thin interlayer improves the output current and transconductance, implying further unpinning of the GaAs surface Fermi level. For the first time, both the dc and RF performance of bottom-up grown planar III-V NW array-based HEMTs are reported. Figure 5 shows the HEMT structure which is achieved monolithically in a single MOCVD growth run, by growing the trapezoidal shaped planar GaAs laterally first followed by the carrier supplying Si-doped AlGaAs shell growth. Representative small-signal RF performance of a small and larger NW-HEMT array is shown in Fig. 5 (bottom). Typical frequency response for our NW-HEMT devices were ~5/15 GHz, and the best RF performance was ft/fmax ~6/23 GHz. To our knowledge, these values are the highest reported for any planar, bottom-up device technology. Additionally, our AlGaAs/GaAs NW-HEMTs have record G_(m-ext) performance per wire and achieve near the best frequency performance of all NW technology despite having a relatively large L_g, L_(s-d), dwire, and no gate oxide.

In summary, we have reported on dc/RF characterization of bottom-up scalable array-based NW transistors. Our preliminary results hold extreme promise for further down scaling of the device geometry

to improve access resistance, channel modulation, and gate leakage with high-κ dielectric gate oxide integration for record-high dc/RF performance.

References

[1] X. Miao and X. Li, "Scalable Monolithically Grown AlGaAs-GaAs Planar Nanowire High-Electron-Mobility Transistor," *Ieee Electron Device Letters*, vol. 32, pp. 1227-1229, Sep 2011.

[2] X. Miao, C. Zhang, and X. Li, "Monolithic Barrier-All-Around High Electron Mobility Transistor with Planar GaAs Nanowire Channel," *Nano Letters*, vol. 13, pp. 2548-2552, 2013/06/12 2013.

[3] R. S. Dowdy, D. A. Walko, and X. Li, "Relationship between planar GaAs nanowire growth direction and substrate orientation," *Nanotechnology*, vol. 24, p. 6, Jan 2013.

[4] R. Dowdy, D. A. Walko, S. A. Fortuna, and X. Li, "Realization of Unidirectional Planar GaAs Nanowires on GaAs (110) Substrates," *Electron Device Letters, IEEE*, vol. 33, pp. 522-524, 2012.

[5] S. A. Fortuna and X. L, "GaAs MESFET With a High-Mobility Self-Assembled Planar Nanowire Channel," *Electron Device Letters, IEEE*, vol. 30, pp. 593-595, 2009.

[6] S. A. Fortuna, J. G. Wen, I. S. Chun, and X. L. Li, "Planar GaAs Nanowires on GaAs (100) Substrates: Self-Aligned, Nearly Twin-Defect Free, and Transfer-Printable," *Nano Letters*, vol. 8, pp. 4421-4427, 2008.

[7] R. S. Dowdy, C. Zhang, P. K. Mohseni, S. A. Fortuna, J.-G. Wen, J. J. Coleman, *and X. Li*, "Perturbation of Au-assisted planar GaAs nanowire growth by p-type dopant impurities," *Optical Materials Express*, vol. 3, pp. 1687-1697, 2013/10/01 2013.

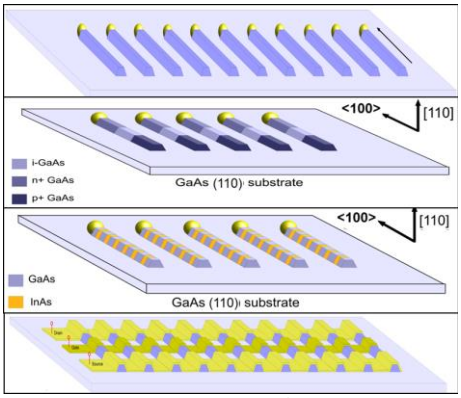

Fig. 1 Development Roadmap of 3D III-V nanowire electronics. Schematic showing from top to bottom: fully aligned VLS planar nanowire array; with lateral p-n junction in GaAs planar nanowires grown on a GaAs (110) substrate; with lateral InAs/GaAs heterojunction; and (d) fully fabricated planar nanowire (with trapezoidal cross-section) array three-terminal FETs.

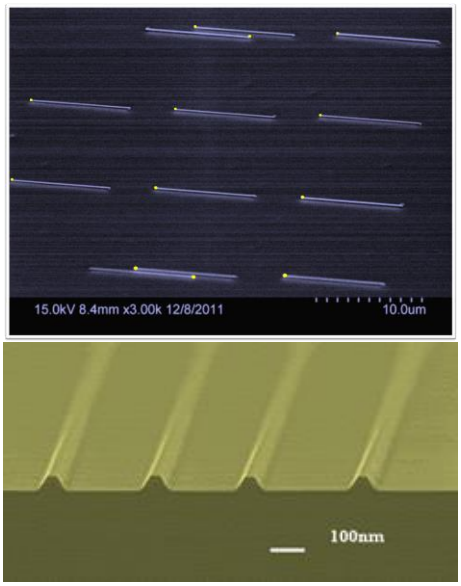

Fig. 2 Site SEM images of self-aligned GaAs planar nanowire array grown out of Au nanoparticles patterned by EBL on a GaAs (100) substrate: (a) tilted top view and (b) cross section.

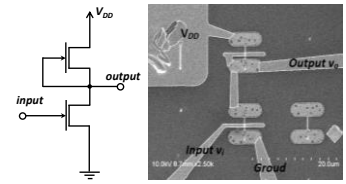

Fig. 3 The left schematic shows the circuit diagram of a simple MESFET amplifier with a current-source load. The SEM image in the middle shows such an amplifier made by two NW MESFETs.

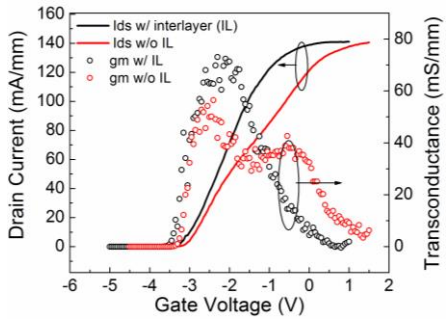

Fig. 4 Planar NW MOSFETs. Comparison of transfer characteristics between MOSFET devices with and without IL. V_{ds}=2 V.

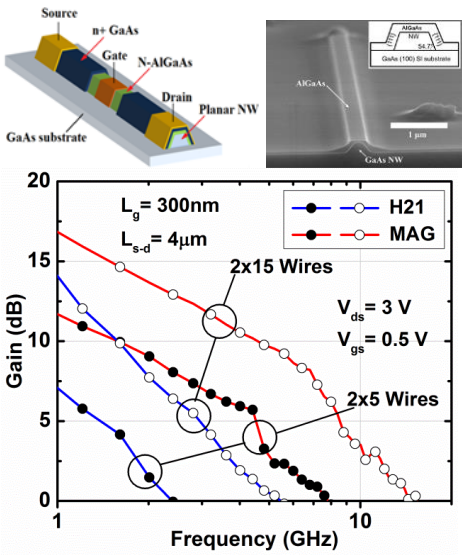

Fig. 5 Planar NW HEMTs. Top: schematic and SEM of planar GaAs NW-AlGaAs HEMT structure. Bottom: Gain versus frequency plot for small (2x5 NWs) and larger (2x15 NWs) NW array HEMTs.