High performance strained GeOI nMOSFETs with in-situ doped epitaxial SiGe stressors

Yuuichi Kamimuta[1], Yoshihiko Moriyama[1], Eiko Mieda[1], Tatsuro Maeda[1], Wipakorn Jevasuwan[1], Yuichi Kurashima[2], Hideki Takagi[2], Minoru Oda[1], Toshifumi Irisawa[1], Keiji Ikeda[1], Etsuo Kurosawa[1] and Tsutomu Tezuka[1]

[1]*Green Nanoelectronics Center (GNC), National Institute of Advanced Industrial Science and Technology (AIST), Japan*

[2]*National Institute of Advanced Industrial Science and Technology (AIST), Japan, E-mail: y-kamimuta@aist.go.jp*

Ge-CMOS devices potentially have advantage in performance as post-14 nm CMOS technology. However, poor Ge nMOSFET performances ever reported stimulates to a shift to Ge pMOS/III-V nMOS CMOS devices rather than all Ge CMOS devices. Realization of high-performance Ge nMOSFETs is a key to implement all Ge CMOS, which has advantage in process costs compared to the Ge/III-V counterparts, into the market. In this paper, for the first time, we demonstrate fabrication of high performance strained GeOI nMOSFETs and demonstrate drive current enhancement due to the strain and low parasitic resistance (R_{para}) with in-situ doped epitaxial n^+SiGe source and drain (S/D) stressors.

Fig. 1 shows a schematic process flow of the device fabrication. GeOI wafers with an Al_2O_3/SiO_2 BOX layers were fabricated by an epitaxial lift-off (ELO) process [1]. The carrier type of GeOI layer is n-type, and the impurity concentration (arsenic) of GeOI layer is about $4\times10^{17}cm^{-2}$, which was confirmed by a SIMS analysis. After the GeOI layers were thinned by wet etching process, SiO_2 dummy gates were formed on the GeOI substrates (**Fig. 1(a)**). n^+Ge or n^+SiGe (x = 0.7, 0.8) layer was epitaxially grown by LP-CVD (**Fig. 1(b)**). Next, Ge active areas were formed by mesa-isolation after removing the SiO_2 dummy gates (**Fig. 1(c)**). After DHF treatment, an Al_2O_3 gate dielectric layer was deposited by ALD process after O_3 passivation. The equivalent oxide thickness (EOT) of the device is about 2.5nm. Then, TaN was deposited as a gate electrode, and then patterned by electron-beam lithography and RIE process (**Fig. 1(d)**). Finally, BEOL process was performed at the maximum temperature of 300 ºC. **Fig. 2** shows a cross sectional TEM image of the GeOI nMOSFET with n^+SiGe (x = 0.7) S/D. GeOI thickness and channel length (L_{ch}) is about 35nm and 60nm, respectively.

First we measured the strain in the GeOI substrate with micro-Raman spectroscopy described in [2]. Raman spectra of the strained GeOI structures are shown in **Fig. 3**. Peaks of Ge–Ge vibration mode in Ge were found to shift toward lower wavenumbers. This result shows that tensile strain is applied in the GeOI channels. **Fig. 4** shows the dummy gate length (L_g) dependence of uniaxial tensile strain in GeOI channel with the SiGe stressors. A maximum value of approximately 0.6 % uniaxial tensile strain was obtained for the device with L_g of 50 nm.

Next, we investigate device characteristics. I_d-V_g characteristics of strained GeOI nMOSFETs with long-channel (L_{ch} = 1μm) are shown in **Fig. 5**. Normal transistor characteristics were confirmed with GeOI nMOSFETs in accumulation mode, thanks to the GeOI thickness (~35 nm) less than the maximum of depletion length (~48 nm). Subtheshold slope (SS) is about 100 mV/dec, and large I_{on}/I_{off} more than $1x10^4$ even though V_d = 1V are obtained. **Fig. 6** shows total resistance (R_{tot}) as a function of various channel length (L_{ch} = 1 ~ 10μm). R_{para} were extracted by y-intercept of this plot. For this plot, the enhancement of channel mobility due to the strain by the n^+SiGe S/D is negligible because L_{ch} is long. R_{para} of the devices are about 2 kΩμm, which are independent of the Ge composition of the n^+SiGe S/D.

L_{ch} dependence of $G_{m,max}$ at V_d = 0.05V are shown in **Fig. 7**. $G_{m,max}$ are increased with decreasing L_{ch} and the Ge composition of the n^+SiGe S/D. The obtained linear $G_{m,max}$ enhancements are reasonable considering the mobility enhancement factors for 0.5% uniaxial tensile strain with L_{ch} of 60nm [3]. L_{ch} dependence of $G_{m,max}$ at V_d = 1V are shown in **Fig. 8**. The enhancement factor are decreased in the saturation region, however, 70% $G_{m,max}$ enhancement is observed over the control device. **Fig. 9** shows I_d-V_g characteristics of the strained GeOI nMOSFET with L_{ch} of 60 nm. **Fig. 10** compares I_d-V_d characteristics of GeOI nMOSFETs with L_{ch} of 60 nm having n^+SiGe (x = 0.7) S/D and n^+Ge S/D. The drive current is 457 μA/μm at V_d = 1V and $V_g - V_{th}$ = 1.5V. **Table 1** shows a comparison of device performances between Ge nMOSFETs previously reported and our work. It is shown that more than 4 times larger drive current has been obtained than the best value ever reported.

In conclusion, high performance strained GeOI nMOSFETs with epitaxial SiGe stressors were demonstrated for the first time. The highest drive current (457 μA/μm at V_d = 1V, V_g-V_{th} = 1.5V) were achieved as a Ge nFETs thanks to the effect of strain and reduced R_{para}. The significant performance enhancement demonstrated is expected to encourage developments on all-Ge CMOS devices.

Acknowledgement: This work was supported by a grant from JSPS through the FIRST Program initiated by CSTP. **References:** [1] T. Maeda et al., *Microelectron. Eng.,* **109** (2013) p.133. [2] Y. Moriyama et. al., *Thin Solid Films,* **520** (2012) 3236. [3] Y. J. Yang et al., *Appl. Phys. Lett.,* **91(10)** (2007) 102103. [4] R. Zhang et al., *IEEE Trans. Electron Devices* **60** (2013) 927. [5] S. H. Hsu et al., *IEDM* (2012) p.525. [6] C. T. Chung et al., *IEDM* (2012) p.383.

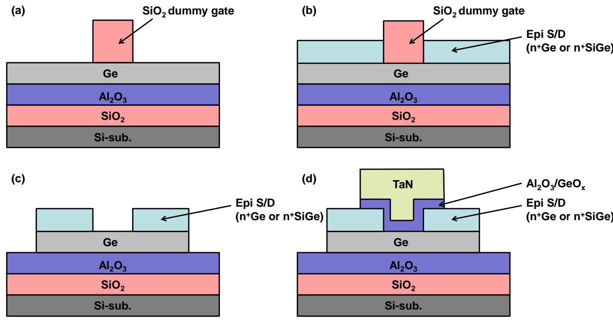

Fig. 1 The schematic process flow of device fabrication.

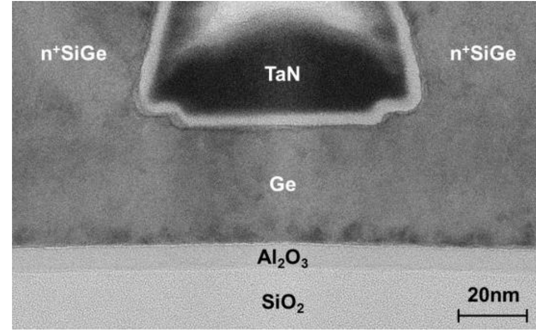

Fig. 2 Cross sectional TEM image of GeOI nMOSFET with n^+SiGe S/D.

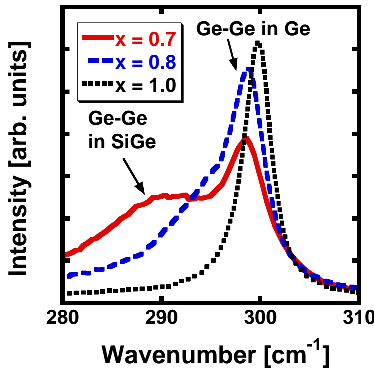

Fig. 3 Raman spectra of strained GeOI structures with SiGe stressors.

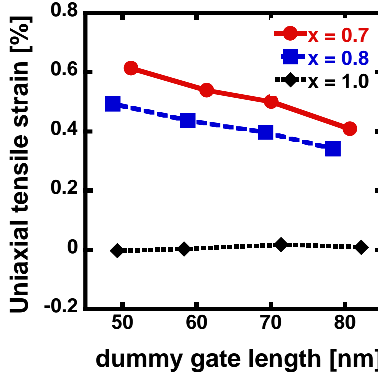

Fig. 4 Uniaxial tensile strain in GeOI channels as a function of L_g with SiGe stressors.

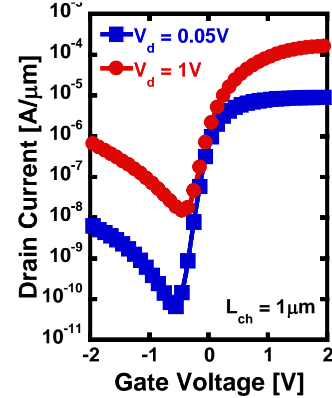

Fig. 5 I_d-V_g characteristics of straind GeOI nMOSFET with L_{ch} of 1μm.

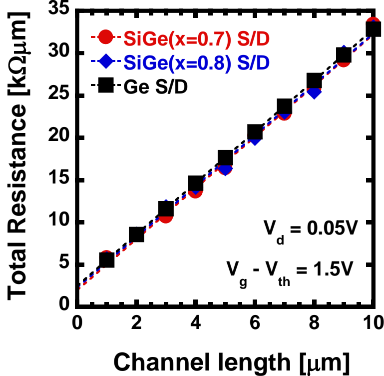

Fig. 6 Relationship between L_{ch} and R_{tot}.

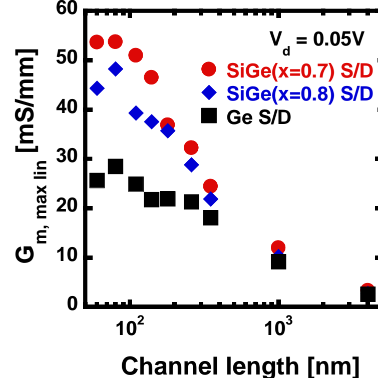

Fig. 7 L_{ch} depencence of $G_{m,\,max}$ in the linear region (V_d = 0.05V).

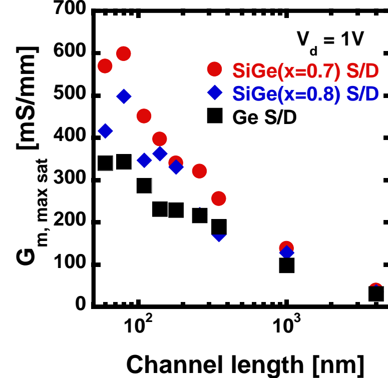

Fig. 8 L_{ch} depencence of $G_{m,\,max}$ in the satulation region (V_d = 1V).

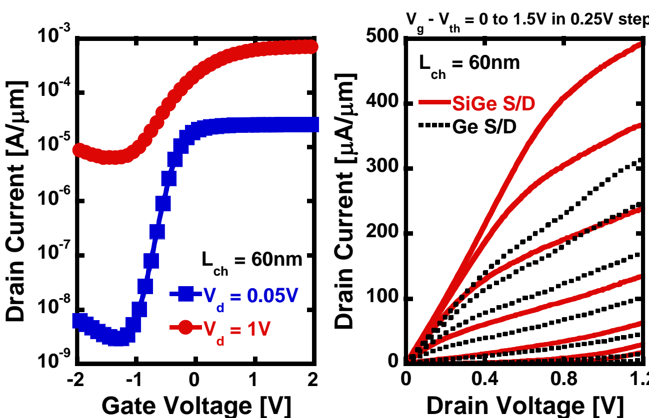

Fig. 9 I_d-V_g characteristics of strained GeOI *n*MOSFET with L_{ch} of 60nm.

Fig. 10 Comparison of I_d-V_d characteristics of GeOI *n*MOSFET with *n*$^+$SiGe (x = 0.7) S/D and *n*$^+$Ge S/D.

Table 1 Comparison of the previous reported Ge *n*MOSFETs and our work.

	Ref. [4]	Ref. [5]	Ref. [6]	This work	
Substrate	Ge bulk	Ge on SOI	Ge on SOI	GeOI	
Structure	Planer	FinFET	GAA	Planer with SiGe stressor	
Dielectric	$HfO_2/Al_2O_3/GeO_x/Ge$	Al_2O_3/GeO_2	Al_2O_3/GeO_2	Al_2O_3/GeO_x	
EOT [nm]	0.76	--	5.5	2.5	
L_{ch} [nm]	5000	120	350	140	60
I_{on} [μA/μm]	12* (V_g-V_{th} = 1V, V_d = 1V)	80 (V_g-V_{th} = 0.9V, V_d = 1V)	110 (V_g-V_{th} = 1.5V, V_d = 1V)	335 (V_g-V_{th} = 1.5V, V_d = 1V)	457 (V_g-V_{th} = 1.5V, V_d = 1V)
DIBL[mV/V]	--	110	--	120	450
I_{on}/I_{off}	~10^3	>10^5	>10^4	~10^4	~10^2
SS [mV/dec]	80	144	94	100	160

*estimated data from I_d-V_d Characteristics