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Multi-Gate MOSFET with Electrically Tunable V_T for Power Management

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Low power SoC applications require multiple threshold voltage (V_T) devices. Typically transistors with three different V_T are offered for such applications. FinFETs show excellent scalability, however setting multiple V_T is challenging due to their undoped/lightly-doped channel. Undoped channel has a number of advantages including high carrier mobility and low random-dopant fluctuations. Vertical nature of the device can increase the drive current per layout area which improves circuit performance [1]. Modulating V_T with body bias is a challenge in FinFETs [2]. Setting multiple V_T in FinFETs is challenging and can be achieved by fin doping doping [3] and/or gate work function. Body bias effect in FinFETs can be improved by optimizing the aspect ratio of fins [4], independent gates [5], or epitaxially-defined channel [6]. Hence it makes sense to retain the vertical nature and the undoped channel in the device while adding the ability to set nominal multiple V_T and dynamic V_T change. *We propose a new vertical multiple-gate MOSFET (Flex-V_T MuGFET) with improved body-bias coefficient, and a new way to set different nominal threshold voltages while keeping the channel undoped.*

The device structure is shown in Fig. 1(a). The device consists of a fin-shaped semiconductor material like silicon. The fin stands on a substrate as in Bulk FinFETs. This forms the 'body' region of the device and is heavily doped. Shallow-trench isolation (STI) is formed to separate the substrate from the successive layers of the device. The body is surrounded by the channel and they are electrically isolated from each other by a thin high bandgap (*High-E_G*) layer material (SiO_2 is used here). The device is finished by forming gate stack, spacers, source-drain epitaxy, source-drain doping, silicidation and contacts. Fig. 1(b) shows the corresponding XY cross-section of the device. The body-insulator-channel forms the back-side MOS structure. Electrostatic potential in the channel and hence its threshold voltage can be modulated by applying a suitable bias to the body.

At a given gate voltage, increasing the body voltage increases the charge (electron) density in the channel, which decreases the threshold voltage of the device. Looking at the conduction and valence band energies [Fig. 2(a)], increasing the body potential causes reduced accumulation in the back side of the channel which increases the electron density in the channel region and hence decreases the threshold voltage [Fig. 2(b)]. Decreasing the high bandgap layer thickness increases the body-to-channel coupling and hence the body-bias coefficient. Threshold voltage of the device increases with decrease in the high bandgap layer thickness [Fig. 3(a)]. *Thickness of the high bandgap layer, which is in the control of the device engineer, is an additional knob to set the threshold voltage of the device*. Once the nominal threshold voltage is set, body voltage can be used to dynamically change the threshold voltage of the device. Threshold voltage can also be set using body doping [Fig. 3]. 6T-SRAM cell using Flex-V_T MuGFET device as the access (AC) transistor shows excellent improvement in Read SNM (~30% at V_{DD}=0.8V) with body bias (V_{BS}) [Fig. 4, Fig. 5]. Improvement in Read SNM comes at the expense of lower Read current. Hence the choice of V_{DD} and V_{BS} should be made considering Read SNM and Read current. Considerable reduction in cell leakage power (up to 40%) is achieved by using the access transistor body voltage [Fig. 6]. Write margin can also be improved (~10%) by applying appropriate body bias [Fig. 7].

There are several possible implementations for the proposed device. In one method, the key is to grow a crystalline oxide on a substrate, and then to grow a semiconductor layer on this oxide. Some of the material systems available in literature are: (a) Si–Perovskite $SrTiO_3$–Si using heteroepitaxy [7], (b) Si–LaYO–Si and Si–LaYO–Ge using solid-phase epitaxy [8], (c) Ge–Pr_2O_3–Si using molecular beam epitaxy [9], (d) Ge–SiO_2–Si using rapid melt growth [10], and (e) inserting oxygen monolayers [11]. Careful design of experiments is required to fabricate the device using one of the abovementioned materials.

References: [1] A.B.Sachid et al, IEDM 2008 pp.1-4; [2] J.Frei et al, IEEE EDL, vol.25, no.12, pp. 813-815, 2004, [3] C.-H.Lin et al, VLSI Tech Symp, pp.15-16, 2012; [4] T.Nagumo et al, IEEE TED, vol.53, no.12, pp.3025-3031, 2006; [5] Y.X.Liu et al, IEDM, pp. 18.8.1- 18.8.3, 2003; [6] S.Mittal et al, DRC, pp.127-128, June 2012; [7] R.A.McKee at al, APL PRL, pp. 3014-3017, Oct 1998; [8] N.A.Bojarczuk at al, Appl. Phy. Lett. , vol.83, no.26, pp.5443,5445, 2003; [9] A.Giussani et al, J. Appl. Phy, vol.105, no.3, pp.033512-6, 2009; [10] J.Feng et al, IEEE EDL vol.27, no.11, pp.911-913, 2006; [11] N.Xu et al, IEDM 2012, pp.6.4.1-6.4.4; [11] Synopsys Sentaurus TCAD Suite 2010; [12] A.B.Sachid et al, IEEE TED, vol.59, no.8, pp.2037-2041, 2012

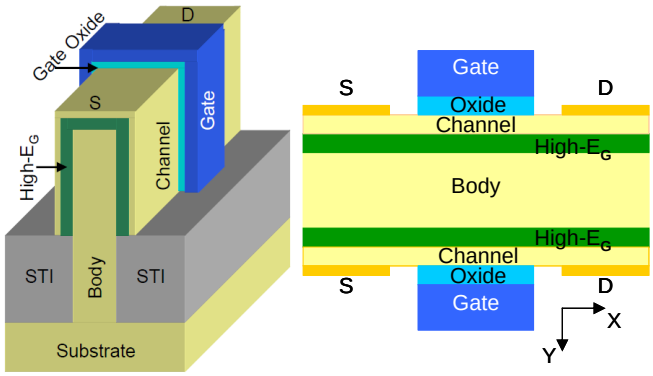
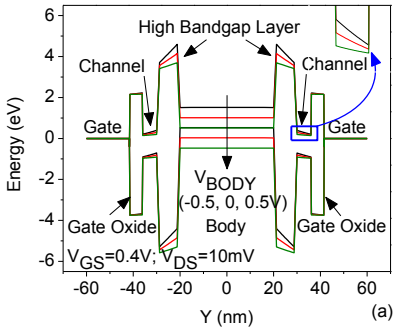


Fig. 1. (a) Device structure (b) Cross-section of the device.

TABLE 1: Device / SRAM Circuit Parameters

Common Parameters	Value
Gate Length (L_G)	20nm
Effective Oxide Thickness (EOT)	1nm
Channel Doping (N_{CH})	$10^{17}cm^{-3}$
S/D Doping (N_{SD})	$10^{20}cm^{-3}$
Gate Work function (NMOS / PMOS)	4.4/4.8eV
Supply Voltage (V_{DD})	0.8V
Flex-V_T MuGFET Parameters	
Channel Thickness (T_{CH})	5nm
Back Oxide Thickness (T_{HEG})	5–20nm
Body Doping (N_{BODY})	$10^{20}cm^{-3}$
SRAM Parameters	
Access Transistor Width (W_{AC})	40nm
Pull Down Transistor Width (W_{PD})	40nm
Pull Up Transistor Width (W_{PU})	40nm



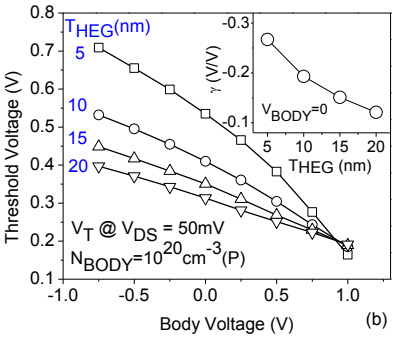


Fig. 2. (a) Conduction and valence bands of the device at the centre of the channel across the fin at different body voltages. (b) Threshold voltage of the device as a function of body voltage for different high bandgap layer thicknesses (T_{HEG})

3D TCAD [12] simulation bench is calibrated against measured data from fabricated FinFETs and is shown in [13]. Physical models used are drift-diffusion formulism are MLDA quantum correction, velocity saturation and overshoot, low field and doping-dependent mobility degradation, carrier generation and recombination, band-to-band tunneling, temperature effects, contact resistance.

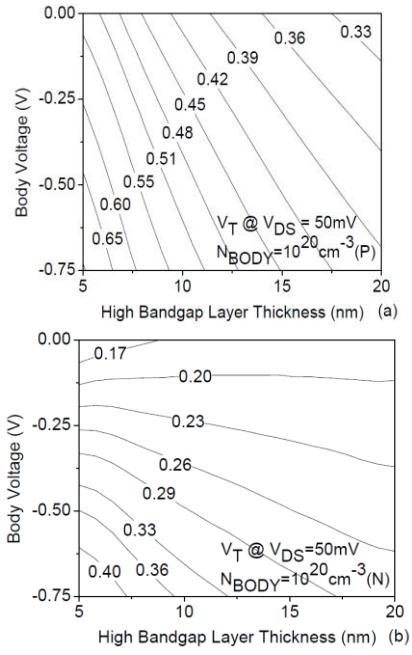


Fig. 3. Impact of high bandgap layer thickness on threshold voltage of the device with (a) P+ body doping of $10^{20}cm^{-3}$ and (b) N+ body doping of $10^{20}cm^{-3}$.

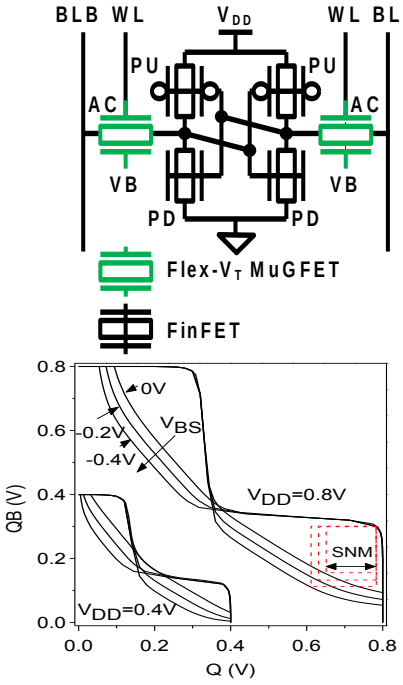


Fig. 4. (a) 6T-SRAM cell using Flex-V_T MuGFET and (b) Butterfly curves for V_{DD}=0.4V and 0.8V for V_{BS}=0V, -0.2V and -0.4V

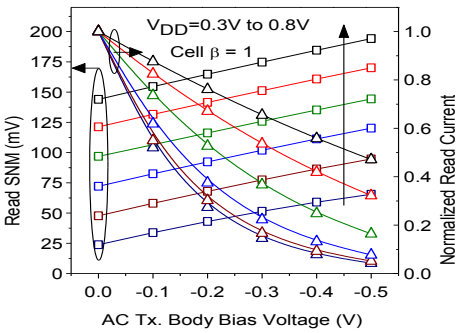


Fig. 5. Impact of body voltage of access (AC) transistor on Read SNM and Read Current (normalized)

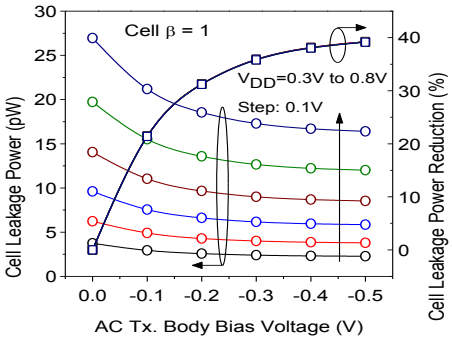


Fig. 6. Impact of body voltage of access (AC) transistor on Cell Leakage Power

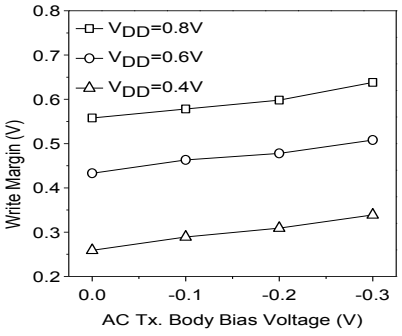


Fig. 7. Impact of body voltage of access (AC) transistor on Write Margin