Student Paper

1/f and White Noise in RF MOSFET Oscillators under Low-Level Signal Injection

Feiran Lei[a] and Marvin H. White[b]

[a] *Department of Electrical and Computer Engineering, The Ohio State University, USA, lei.39@osu.edu,*
[b] *Department of Electrical and Computer Engineering, The Ohio State University, USA.*

Introduction:

Noise generated in electronic devices affects greatly the performance of communication systems. In oscillators, baseband device noise is up-converted to the RF as phase noise – short-term random frequency fluctuations in the output signal. In receivers, phase noise limits the signal-to-noise ratio (SNR), bit-error-rate (BER), introduces reciprocal mixing with strong interferers and, in a transmitter, corrupts nearby receivers. We use an external low-level injection signal to synchronize an oscillator [Synchronous Oscillator (SO)], which tracks the reference signal and reduces the phase noise of the system [2-3]. We develop a relationship between device baseband noise and an oscillators' RF phase noise and introduce a noise shaping function to describe signal injection into a differential delay-line SO with active inductor-like loads to achieve suppression of the SO phase noise.

Delay Line Phase Noise Modeling

Fig. 1 shows a single delay cell with MOS differential pair M3 and M4, a MOS tail current source M2 (Iss), and active inductor loads M5 M7 and M6 M8. Active inductor loads minimize parasitic capacitance at the output node for high speed operation. PMOS pull up latches M9 and M10 allow the oscillator to achieve a nearly rail to rail swing as shown in Fig. 2 for $V_{DD} = 1.2V$. The actual voltage swing Vos has a voltage loss due to the voltage drop across the tail current Iss.

(a) 1/f Noise: 1/f noise fluctuates at a rate much lower than the oscillating frequency. The dominant source of 1/f noise in the differential delay cell resides in M1, which drives the tail current and is amplified in the delay stage. Since fluctuations in each tail current are uncorrelated, the delay variations will accumulate and create significant phase noise. The 1/f noise is modeled as a current source $\bar{\iota}^2_{n\_1/f}$ shown in Fig.1. The expression for the power spectral density (PSD) of the M1 drain current noise is introduced in [1] as

$$S_{I_{n\_1/f}}(f) = \eta \cdot \frac{I_{D1}^2}{f} \qquad (1)$$

where $\eta = \frac{k_B T}{W_1 L}\left[\frac{1}{N_n} + (\alpha + \beta)\mu\right]^2 \frac{\rho_t}{\lambda}$ describes noise contribution with fluctuations in free carriers N_n^{-1} and mobility $(\alpha + \beta)\mu$. α models Coulomb scattering, β surface roughness, λ 'tunneling' attenuation, while ρ_t is the gate stack volume trap density. The PSD, dominated by M1, is

$$S_{I_{SS}}(f) = \eta \cdot \frac{I_{SS}^2}{f} \qquad (2)$$

For the differential delay-line oscillator, the loads may be described by a RC circuit [6] with propagation delay and free running frequency $t_d = C_{eff}V_{os}/I_{SS} = R_{eff}C_{eff}$ and $f_o = 1/2Nt_d$, respectively, where N is the number of delay stages. The sensitivity of the frequency to tail current is $s_{I_{SS}} = \frac{\partial f_o}{\partial I_{SS}} = \frac{f_o}{I_{SS}}$, which gives $S_{f_o}(f) = s_{I_{SS}}^2 \cdot S_{I_{SS}}(f) = \frac{\eta \cdot f_o^2}{f}$ and with a narrowband expression [4] the output phase noise at an offset frequency of Δf_{os} is

$$\mathcal{L}_{1/f}(\Delta f_{os}) = \frac{S_{f_o}(\Delta f_{os})}{4\Delta f_{os}^2} = \frac{\eta \cdot f_o^2}{4\Delta f_{os}^3} \qquad (3)$$

(b)Thermal Noise: The period jitter $\sigma^2_{T\_white}$ due to white noise can be found as 2N multiplying the ratio between the output noise voltage and the slope of the differential switching voltage at zero-crossing [5]. For a simplified case, assume only three white noise sources dominating the total phase noise: 1) white noise due to the effective load resistor R_{eff}; 2) tail current noise $\bar{\iota}^2_{n\_tail}$ from the tail NMOS M2 during transition time; and 3) current noise $\bar{\iota}^2_{n\_diff}$ from the differential pair M3 and M4 during transition time. Thus, the period jitter can be calculated by the formula:

$$\sigma^2_{white} = 2N\sigma^2_{td} = 2N\frac{\bar{v}_n^2}{(I_{SS}/C_{eff})^2} = 2N\frac{C_{eff}^2}{I_{SS}^2}\left[\frac{2k_B T}{C_{eff}} + \frac{2k_B T\gamma g_{m2}R_{eff}}{\pi C_{eff}} + \frac{3k_B T\gamma g_{m3,4}R_{eff}}{2C_{eff}}\right] \qquad (4)$$

The relationship between the period jitter and the phase noise can be expressed as [5]:

$$\mathcal{L}_{\text{white}}(\Delta f_{os}) = \sigma^2_{T\_\text{white}} \frac{f_o^3}{\Delta f_{os}^2} = \frac{1}{(2NR_{\text{eff}}C_{\text{eff}}I_{SS})^2}\left[\frac{2k_BT}{R_{\text{eff}}} + \frac{2k_BT\gamma g_{m2}}{\pi} + \frac{3k_BT\gamma g_{m3,4}}{2}\right] \cdot \frac{1}{\Delta f_{os}^2} \qquad (5)$$

Injection Locked SO: The phase noise of the SO in Fig. 3 is reduced substantially by an injection of a low-noise reference to the oscillator, which intuitively can correct the zero-crossing of the output waveform in each period in the time domain, thereby, reducing the jitter accumulation at the output. The noise shaping function with injection is

$$\mathcal{L}_\Delta(\Delta f_{os}) = 10\log\frac{\Delta f_{os}^2}{(K_{SO}^2 - \Delta f^2) + \Delta f_{os}^2} \qquad (6)$$

where K_{SO} is an injection parameter which is also half the SO tracking bandwidth [3]. Δf is the frequency difference between injection frequency and oscillator free running frequency (f_o =3.45GHz). Fig.4 shows the phase noise in the free running oscillator as well as in the SO system. Device baseband 1/f noise is up-converted to high frequency regime with a slope of $1/f^3$ (-30dB/dec) while device baseband white noise is up-converted to high frequency regime with a slope of $1/f^2$ (-20dB/dec). The SO system reduces the phase noise in the low frequency offset region within the SO tracking bandwidth (30 dB suppression at Δf_{os} = 100 KHz).
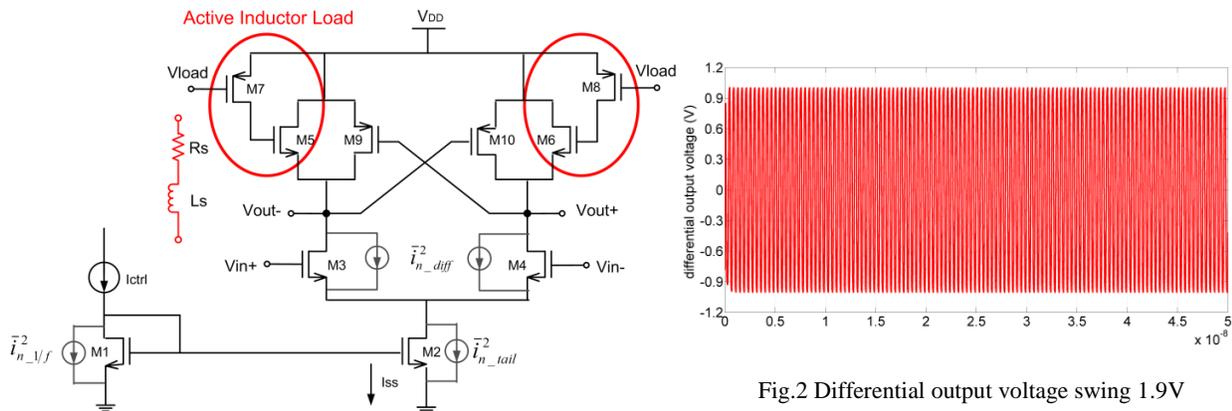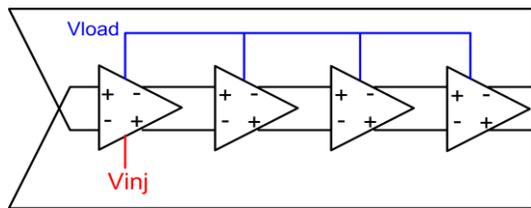

Fig.1 Differential delay cell with current noise model

Fig.2 Differential output voltage swing 1.9V

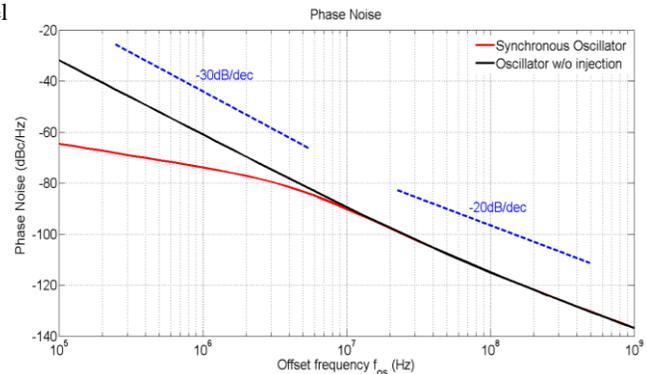Fig.3 Synchronous Oscillator (SO) with Injection to reduce the oscillator phase noise

Fig.4 Phase Noise at RF (f_o=3.45GHz) and up-converted 1/f and white noise. Phase Noise (Δf_{os}=100 KHz) suppressed by 30 dB

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