Discrete Time Parametric Amplifier based Dynamic clocked Comparator

Hitesh Shrimali

Department of Physics, Università degli Studi di Milano, Italy, hitesh.shrimali@unimi.it

A low gain discrete-time parametric amplifier (DTPA) [1] can sample, hold and amplify an input signal using the MOS varactor properties. The DTPA consumes ultra low power with very low noise. A DTPA exhibits a common-mode voltage shift at the output terminal. To nullify this common-mode voltage shift, [2] has proposed a complementary parametric amplifier (CDTPA). In a CDTPA, an nMOS-DTPA and a pMOS-DTPA act as loads to each other. In [2], a gain-boosted double complementary parametric amplifier (DCDTPA) has been proposed. The gain boosting in a DCDTPA is achieved through a reverse connected parametric amplifier (RDTPA). Fig. 1 shows the schematic diagrams of the DTPA, the CDTPA and the RDTPA. A charge transfer amplifier (CTA) has been designed in [3] as a pre-amplifier stage of the dynamic clocked comparator. The demonstration of a nullified common-mode output voltage shift for a DTPA based comparator has been implemented in [4], [5]. This work proposes the common-mode voltage nullification scheme for the dynamic clocked comparator across the varying process, voltage and temperature. Fig. 2 shows the Q-V characteristics of the anti-parallel connected parametric amplifiers whose common mode voltage shift is nullified. Using this principle, an RDTPA was used as a pre-amplifier stage of the proposed comparator. The level shifter scheme to nullify an input common mode voltage (V_{CMI}) shows minimal deviation for varying process corners as the level shift is compensated through the same devices i.e. nDTPA tunes for nRDTPA and pDTPA tunes for pRDTPA. Fig. 3 shows the proposed preamplifier stage used as the input stage of the dynamic latch. The complete design including the latch and the RDTPA is designed in a standard 32 nm CMOS technology with the supply voltage of 1 V and a sampling frequency of 50 MSPs. Fig. 4 shows the Monte-Carlo simulation results for the proposed comparator for 1000 runs. It shows ±4 mV of the input offset voltage (*IOV*). Fig. 5 shows the microchip photograph of the dynamic clocked comparator including the pre-amplifier, the clock generator circuit and the output buffers. The overall circuit consumes an area of 25 µm X 40 µm. The DTPA based dynamic clocked comparator was characterized in the laboratory. The laboratory test setup block diagram is shown in Fig. 6. The base clock was generated by an Agilent function generator 8113A; the input single generated by an Agilent 33220A; the DC voltages such as V_{CMI} and VDD are generated by the Agilent 6611C DC source; the output of the comparator was observed on an Agilent digital storage oscilloscope MSO9104A. Thermonics' precision forcing system T-2800 was used to check the circuit performance under various temperatures viz. -40 °C, 25 °C and 125 °C. Fig. 7 shows the variation of *IOV* with respect to V_{CMI} . The experiment has been performed for ±10 % variation of VDD and for the temperatures of -40 °C, 25 °C and 125 °C. During this experiment, one of the inputs of the comparator has been fixed at VDD/2 and the other input is kept as a sweeping parameter. The plot shows relatively constant *IOV* around the point VDD/2 (Fig. 2). The measurement results show 7 mV of an input offset voltage at a typical corner. The proposed comparator consumes 120 µW of power and shows 15 ns of regeneration time with 2.4 pJ of energy efficiency. Fig. 15 shows the output response of the comparator when the applied voltage at IN terminal is VDD/2 + 50 mV (with a finite time delay) and the reference voltage is kept at VDD/2, keeping the signal frequency at 50 MHz. The regeneration time depends on the regeneration time of the complete circuit including the chain of buffers at the output of an amplifier. The regeneration time constant is given by $C_L=g_m$. Where g_m is the transconductance of the CMOS inverter. A large capacitive load of 10 pF limits the speed of the comparator.

Acknowledgements

This work has been carried out at STMicroelectroelectronics, Greater Noida, India. The author would like to thank Chandrajit Debnath, Rakesh Malik and Shubham Gupta of STMicroelectronics for their support. The author would also like to acknowledge Dr.Shouri Chatterjee of Indian Institute of Technology of Delhi for his expert valuable comments.

References

[1] S. Ranganathan and Y. Tsividis, "Discrete-time parametric amplification based on a three-terminal MOS varactor: analysis and experimental result," IEEE Journal of Solid-State Circuits, vol. 38, no. 12, pp. 2087–2093, Dec. 2003.
[2] A. Yoshizawa and S. Lida, "A gain-boosted discrete-time charge domain FIR LPF with double-complementary MOS parametric amplifiers," in Digest of Technical Papers. IEEE International Solid-State Circuits Conference, 2008. ISSCC 2008., Feb. 2008, pp. 68 –596.
[3] K. Kotani, T. Shibata, and T. Ohmi, "CMOS charge-transfer preamplifier for offset-fluctuation cancellation in low-power A/D converters," IEEE Journal of Solid-State Circuits, vol. 33, no. 5, pp. 762 – 769, May. 1998.
[4] J. Oliveira, J. Goes, N. Paulino, and J. Fernandes, "Improved low power low-voltage CMOS comparator for 4-bit flash ADCs for UWB applications," in 14th International Conference on Mixed Design of Integrated Circuits and Systems, 2007 (MIXDES '07), Jun. 2007, pp. 293 –296.
[5] J. Oliveira, J. Goes, M. Figueiredo, E. Santin, J. Fernandes, and J. Ferreira, "An 8-bit 120-MS/s interleaved CMOS pipeline ADC based on MOS parametric amplification," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 57, no. 2, pp. 105 –109, Feb. 2010.

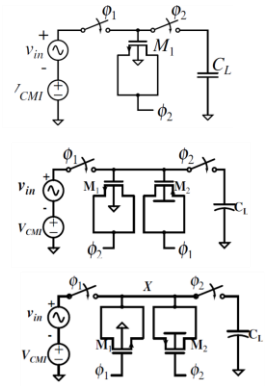


Fig.1 The schematic diagrams of proposed preamplifier stage for the dynamic DTPA, CDTPA and RDTPA.

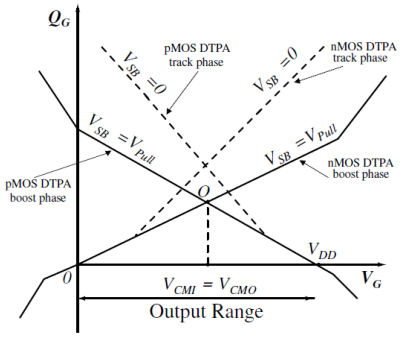


Fig. 2 The Q-V characteristics of the anti-parallel connected parametric amplifier.

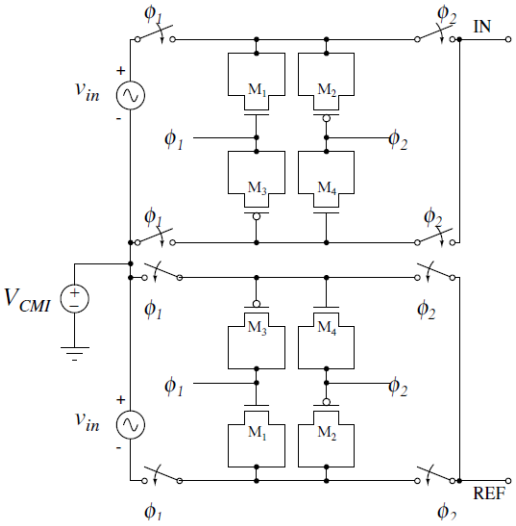


Fig.3 The clocked comparator.

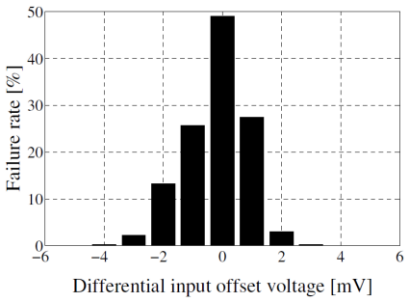


Fig. 4 Monte-Carlo Simulation for N= 1000.

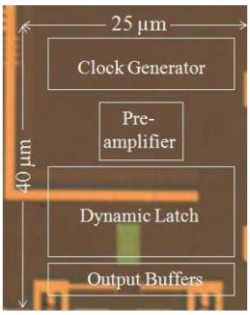


Fig.5 Microchip photograph.

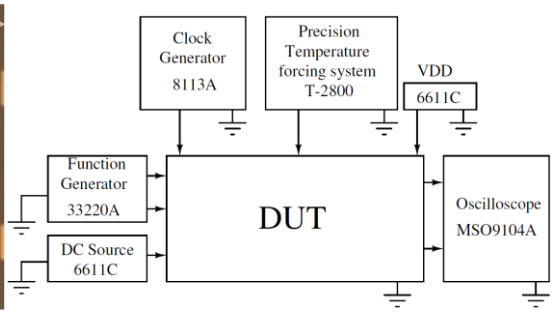
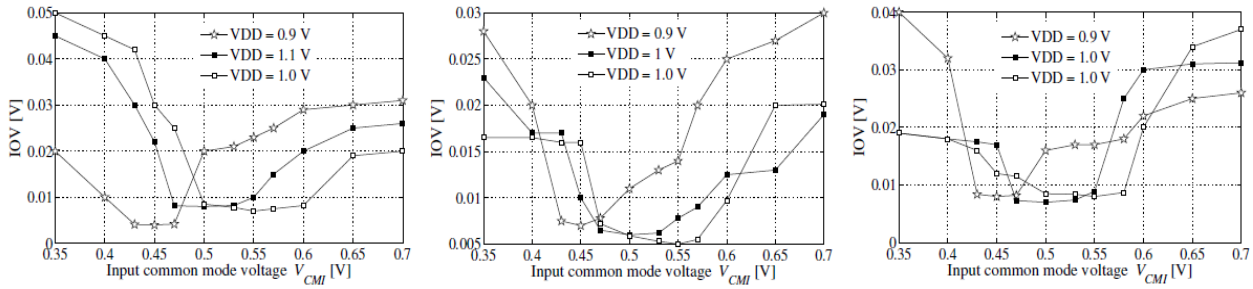


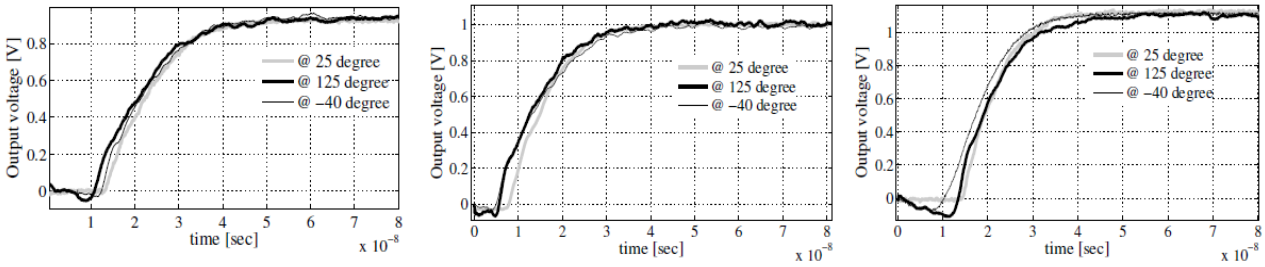
Fig. 6 Test setup.



(a) **(b)**

(c)

Fig. 7 The variation of an *IOV* with respect to V_{CMI} at (a) 125 ◦C (b) 25 ◦C and (c) -40 ◦C (considering ± 10% variation in VDD).



(a) **(b)**

(c)

Fig. 8 The output response of the proposed comparator for a differential input signal of 50 mV for a VDD of (a) 0.9 V, (b) 1.0 V and (c) 1.1 V (under the temperature of -40 ◦C, 25 ◦C and 125 ◦C).