Student Paper

A New T-Shaped Source/Drain Extension (T-SSDE) Gate Underlap GAA MOSFET with Enhanced Subthreshold Analog/RF Performance for Low Power Applications

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In recent years aggressive scaling of the MOS device dimensions and concomitant enhancement of cut off frequency attracted immense possibilities of MOS devices for low power and Radio Frequency regime. The subthreshold operation of MOS devices made them a strong candidate for analog applications due to high gain by improving the transconductance generation factor (TGF, g_m/I_{DS}). However reduction in gate length manifest the short-channel effects (SCEs), hot carrier effects, punch trough and DIBL. So the strong solution of gate length reduction in 10 nm gate length regime is Gate All Around (GAA) MOSFET. GAA provides ultimate electrostatic gate control over the channel. Beside it, a small silicon pillar radius causes carrier mobility degradation that offset the benefits of scaling [1].

To overcome these setbacks a non-classical MOSFET structure has been developed to improve the electrical and high frequency characteristics of the MOS devices. The gate underlap structure reduces SCEs very effectively in GAA MOSFET via gate bias-dependent effective channel length (L_{eff}). the effective channel length in subthreshold region is almost equal to the gate length in the case of strong inversion. Gate underlap architecture also eliminates the gate induced drain leakage (GIDL) with reduction in gate to source and gate to drain fringing capacitance. It also reduces gate-source/drain tunneling current. These numerous advantages enhances the device performance in terms of higher speed and reduced dynamic power consumption & makes it prominent device for digital circuits . But the underlap gate structure suffers from reduced on current (I_{on}) and increased Source/Drain (S/D) series resistance [2]. High series resistance due to the small contact area of source/drain region forming abrupt Source/Drain junctions is another technology bottleneck of these extremely scaled MOS devices that employs several challenges on doping techniques and thermal budget.

A new T-Shaped Source/Drain Extension (T-SSDE) Gate Underlap GAA MOSFET is proposed to remove the problem of reduced Ion and increased series S/D resistance in this paper. This approach does not increase the total area of the device. Proposed device enhances figure of merits (FOM's) like I_{on}, g_m, g_d, I_{on}/I_{off} ratio etc,. The device will be analyzed and superiority of T-SSDE Gate Underlap GAA MOSFET over Underlap GAA MOSFET will be established. The comparative results of proposed device with underlap GAA MOSFET device, obtained from ATLAS 3-D Device simulator [3] will be discussed.

References

[1] L. Zang, C. Ma, J. He, X. Lin, and M. Chan, "Analytical solution of subthreshold channel potential of gate underlap cylinderical gate-all-around MOSFET ," *Solid-State Electronics*, vol. 54, pp. 806-808, April 2010.

[2] K. Koley, A. Dutta, B. Syamal, S. K. Saha, and C. K. Sarkar, "Subthreshold Analog/RF Performance Enhancement of Underlap DG FETs With High-k Spacer for Low Power Applications," *IEEE Trans. Electron Devices*, vol. 60, no. 1, pp. 63-69, January 2013.

[3] ATLAS User's Manual: 3-D Device Simulator, Silvaco Inc., Santa Clara, CA, USA, 2012.

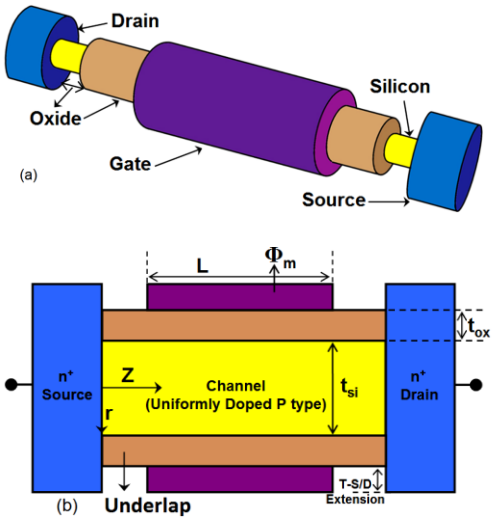

Figure.1 (a) 3-D schematic view of T-SSDE Gate Underlap GAA MOSFET (b) Cross sectional view of T-SSDE Gate Underlap GAA MOSFET, Channel length L = 30 nm, Diameter of Si pillar t_{Si} = 10 nm , T-SSD Extension Diameter = 12 nm, p-type substrate doping N_A =1 × 10^{16} cm^{-3}, N_D = 1 × 10^{18} cm^{-3}, SiO_2 thickness t_{ox}, work-function of the metal gate electrode Φ_m, dielectric permittivity of SiO_2 is ε_{ox}.

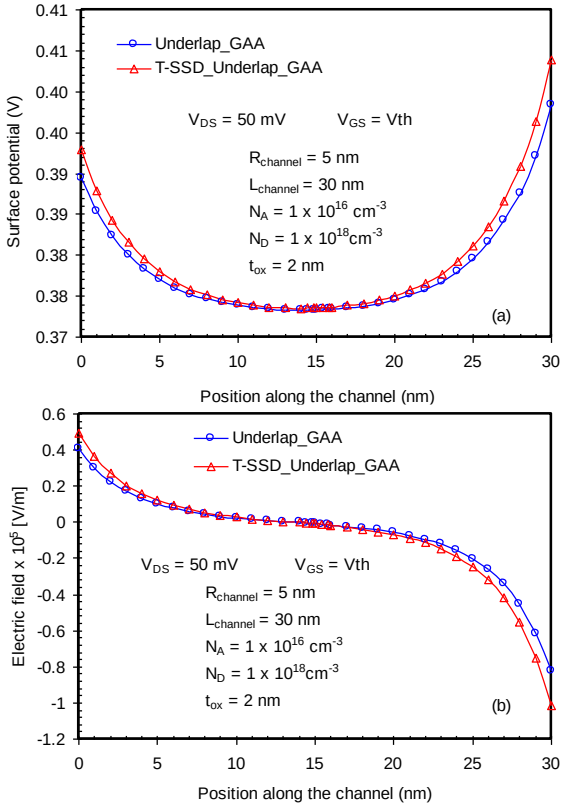

Figure.2 (a) Variation of surface potential as a function of position along the channel of T-SSDE Gate Underlap GAA MOSFET. Fig. (b) Variation of electric field as a function of position along the channel of T-SSDE Gate Underlap GAA MOSFET, Channel length L = 30 nm, Diameter of Si pillar t_{Si} = 10 nm, work-function of the metal gate electrode Φ_m = 4.8 eV (optimized), dielectric permittivity of SiO_2 is ε_{ox} = 3.9.

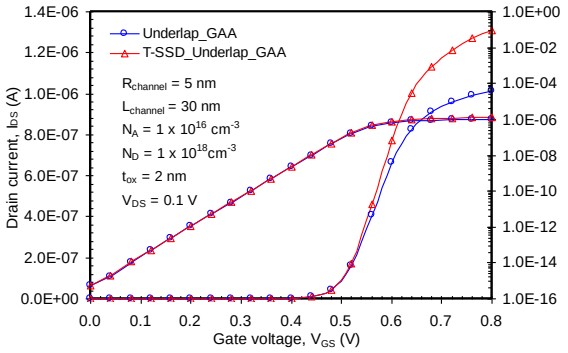

Figure. 3 Variation of drain current (I_{DS}) as a function of applied gate bias (V_{GS}) at applied drain voltage (V_{DS} = 0.1 V) of T-SSDE Gate Underlap GAA MOSFET. Channel length L = 30 nm, Diameter of Si pillar t_{Si} = 10 nm , T-SSD Extension Diameter = 12 nm, p-type substrate doping N_A = 1 × 10^{16} cm^{-3}, N_D = 1 × 10^{18} cm^{-3}, SiO_2 thickness t_{ox}, work-function of the metal gate electrode Φ_m = 4.8 eV, dielectric permittivity of SiO_2 is ε_{ox} = 3.9.

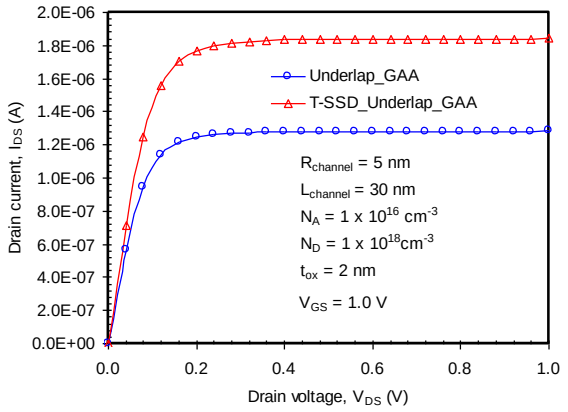

Figure. 4 Variation of drain current (I_{DS}) as a function of applied drain bias (V_{DS}) at applied gate voltage (V_{GS} = 1.0 V) of T-SSDE Gate Underlap GAA MOSFET.

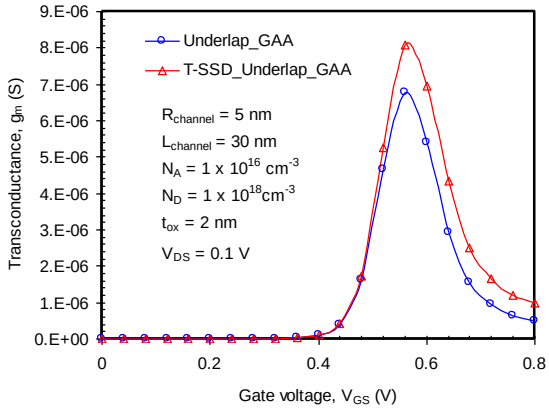

Figure. 5 Variation of transconductance(g_m) as a function of applied gate bias (V_{GS}) at applied drain voltage (V_{DS} = 0.1 V) of T-SSDE Gate Underlap GAA MOSFET, N_A =1 × 10^{16} cm^{-3}, N_D = 1 × 10^{18} cm^{-3}, SiO_2 thickness t_{ox}, work-function of the metal gate electrode Φ_m = 4.8 eV, dielectric permittivity of SiO_2 is ε_{ox} = 3.9.