Suppression of Gate-Induced Drain Leakage Current in Junctionless GOI MOSFETs

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With an increase in demand for high speed and/or low power operation of CMOS devices, high mobility channel MOSFETs, such as Ge MOSFETs, for instance, are being intensively investigated [1]. It is required to suppress off-state leakage current (I_{OFF}) in order to reduce power consumption. Although high current drivability is expected for Ge MOSFETs, large gate-induced drain leakage (GIDL) current is foreseen due to a narrow band gap. Therefore, suppression of GIDL is indispensable in order to suppress I_{OFF} in Ge MOSFETs. Junctionless transistors (JLTs) are expected to have good cut-off characteristics because of suppressed DIBL and SS [2, 3]. Recently, a low I_{OFF} value less than 1 nA/μm have been reported for a poly-Ge tri-gate p-JLT which showed suppressed GIDL characteristics [2]. In this paper, electrical characteristics of planar JLTs with a Ge-on-insulator (GOI) structure are simulated and are compared with junction-source-and-drain transistors (JSDTs) from a viewpoint of I_{OFF}.

Device structures of JLT and JSDT are schematically shown in Fig. 1. Both JLT and JSDT have an identical structure except for extension regions, which was assumed only for JSDT, and impurity type and concentration in the channel region. A thickness of offset spacers was set to a thinnest value (44 nm) which satisfies a condition of $I_{ON}/I_{OFF} > 10^4$ for JSDT. Here, I_{OFF} is defined by 10 times of a minimum value of I_D and I_{ON} is defined by I_D at $V_G = V_{G0} + V_{DD}$, where V_{G0} is V_G at which $I_D = I_{OFF}$ and $V_{DD} = 1$ V. I_D-V_G characteristics were calculated for the GOI nMOSFETs (Fig. 2) using a device simulator HyENEXSS^{TM} with a non-local band-to-band-tunneling (BTBT) model [4, 5]. The calculated results show that GIDL is more suppressed in JLTs than in the JSDT except for a JLT having impurity concentration in the channel region (N_{CH}) of $1x10^{19}$ cm^{-3}, where GIDL shows a strange behavior that it decreases as V_G decreases. Sub-threshold current for JLT having N_{CH} of $1x10^{19}$ cm^{-3} is considered to be mainly due to not BTBT but punch-through because it is carried mainly by electron even under the gate electrode. Also for Ge-channel pMOSFETs, qualitatively equivalent results were obtained. In the followings, only JLTs having N_{CH} of less than or equal to $1x10^{18}$ cm^{-3} and JSDT are considered. The reason for the suppression of GIDL can be understood by a weaker electrical field along channel length direction (E_X) in JLTs than that in JSDT. (Figs. 3 and 4) Lengths of a region between the gate and the source/drain, where profiles of electrical potential are not flat, are longer in JLTs than that in JSDT (Fig. 5) due to the fact that extension regions, where impurity concentration is higher than that in channel region, were assumed only for JSDT. Hence, the reason for the weaker E_X in JLTs than that in JSDT can be understood by a longer "effective offset length" (EOL). Therefore, it is expected that thickness of offset spacers can be set thinner and that higher I_{ON} is realized for JLTs than for JSDTs under a condition of fixed I_{OFF}. I_{ON}-I_{OFF} relationships were calculated for JLTs having offset spacers of a thickness of 24 to 44 nm (5 nm step) and JSDTs having that of 34 to 54 nm (5 nm step), corresponding to approximately identical EOL for both JLTs and JSDTs. It is shown that I_{ON} is higher under a condition of fixed I_{OFF} for JLTs than JSDTs. (Fig. 6) This result can be understood by the fact that carrier concentration underneath the offset spacers is higher for JLTs than JSDTs because the region is doped by donors for JLTs while it is doped by acceptors for JSDTs. The lower I_{ON} values than those for state-of-the-art Si-pMOSFETs are due to high parasitic resistance of the GOI layers as thin as 2 nm which is required to suppress the short channel effects (SCE). Introduction of 3-dimensional structures, such as a tri-gate structure for instance, are promising to increase current drivability because a thicker channel is allowed with suppressing SCE.

In conclusion, junctionless transistors potentially have an advantage in I_{ON}-I_{OFF} characteristics over conventional inversion-type MOSFETs due to the lower GIDL current.

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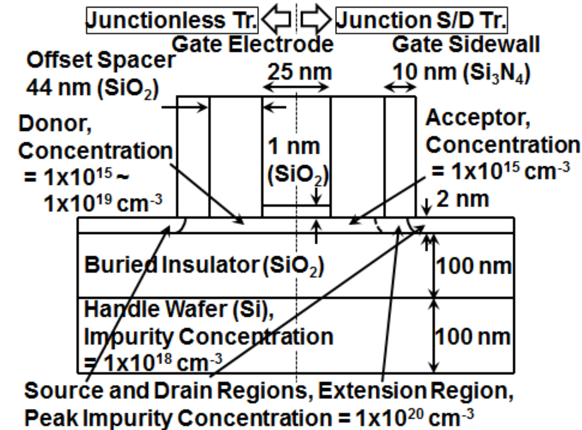

Fig. 1. Structures of nMOSFETs in this study. Both devices have a symmetrical structure under an exchange of source and drain.

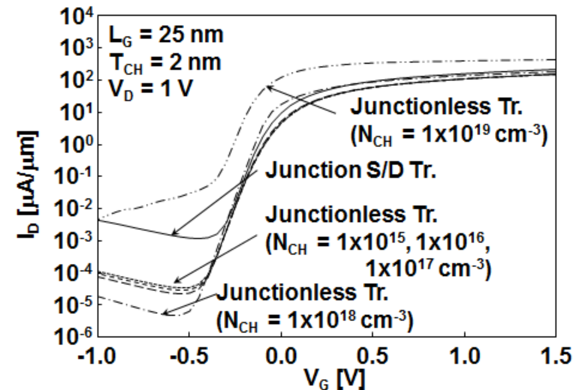

Fig. 2. I_D-V_G characteristics for nMOSFETs. Here, L_G = 25 nm and V_D = 1 V.

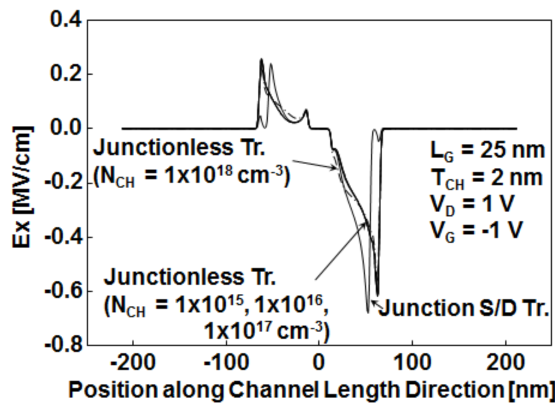

Fig. 3. Profiles of electrical field strength along channel length direction. Here, $V_D = -V_G = 1$ V.

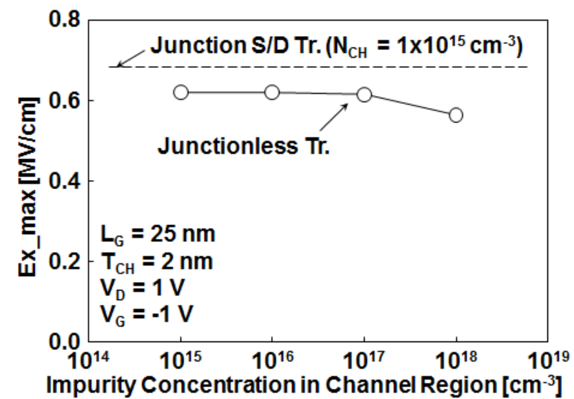

Fig. 4. Dependence of maximum electrical field strength on impurity concentration in channel region. Here, $V_D = -V_G = 1$ V.

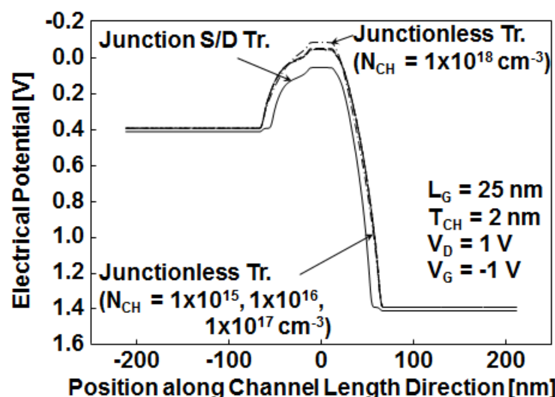

Fig. 5. Profiles of electrical potential along channel length direction. Here, $V_D = -V_G = 1$ V.

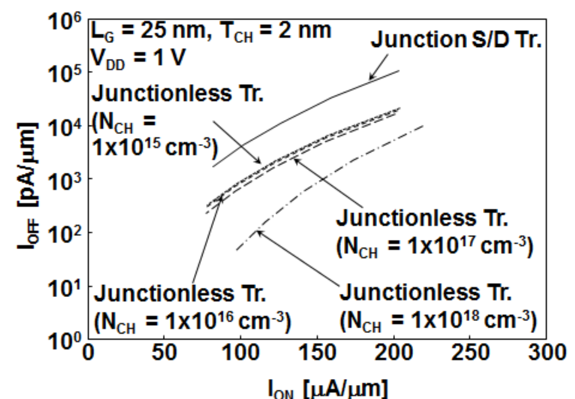

Fig. 6. Relationships between I_{ON} and I_{OFF}. Here, V_{DD} = 1 V.