Student Paper

The Variational Thermodynamic Modeling of Reverse Bias Capacitance Voltage Characteristics of an Isolated Silicon p-n Junction

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The p-n junction is foundational to solid state electronics. The usual model for the pn junction in standard textbooks relies on the depletion approximation (DA) and plane geometry [1]. In this paper, we have applied our Variational Thermodynamic (VT) methodology [2-3], also within these confines, in order to confirm that our approach is fully equivalent to the standard method. We then proceed to model the effect of mobile charges. The effect of mobile charges within the depletion increases the capacitance of the device. This increase will in turn increase the RC time constant and thus decrease the switching speed and increase the internal heating. Both of these effects are important considerations for design of devices.

The schematic of the junction we model using VT is shown in Fig. 1. The potential trial functions we use for the p and n regions are shown in Fig. 2. Here, our trial functions are simple one-dimensional Cartesian expressions which ignore fringe field effects and non-ideal fabrication outcomes. With these assumptions, the flow of our methodology is elaborated in Fig. 3. A crucial part of the flow requires choosing potential trial functions which should approximate solution to the Euler Lagrange (E-L) equation of the variational principle, be continuous, satisfy the boundary conditions and be formulated with parameters which will allow the variational principle to be evaluated and subsequently minimized. The methodology starts by defining the Helmholtz Free Energy (F) which consists of capacitive and charge energy in the appropriate regions of the device. The capacitive energy is found using the trial functions (Fig. 2) and the assumed fixed and mobile charge distributions shown in Fig. 4. We model the mobile charges assuming linear variation of the logarithm of the charge densities [4].

Of special interest is how the junction responds to application of reverse bias. In Fig.5, we show our result for the p and n depletion widths, w_p and w_n respectively, as functions of reverse bias. In Fig. 6, we show the resulting potential distribution in the space charge region for sample values of reverse bias. We have measured the reverse bias C-V of a real p-n diode (IXYS DSEI30-06A, 600V, 30A) using a Keithley Model 4200 semiconductor characterization system. In Fig. 7, we compare the variation of the measured capacitance as a function of applied reverse bias with those from our model, at first using only DA and then including mobile charges. The capacitance predicted by our VT model considering mobile charges is closer to the measured capacitance compared to that of the DA case. The model capacitance, which assumes no leakage current, deviates from that of the measured values at large reverse bias.

References:

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Figure 3: Variational Thermodynamic Methodology flow for reverse-biased capacitance of a p-n junction.



Figure 4: (a) Fixed charge and (b) electron (red) and hole (blue) charge distributions in the space charge region.



Figure 6: Potential in the space charge region calculated by our model, showing w_p, w_n, φ_{op} and φ_{on} magnitudes.



Figure 5: w_p and w_n for p and n regions vs. reverse-biased voltage, V_R .



Figure 7: Measured (blue) C-V characteristics of the p-n junction under reverse bias with our model under DA (yellow) and our model including mobiles charges (red).