Student Paper

Analysis of Heat Dissipation of Epitaxial Graphene Devices on SiC

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Various demonstrations of graphene rf transistors have proven graphene's potential for high frequency applications, based on outstanding carrier mobility, high saturation velocity and high carrier density[1, 2]. Intense electric fields and high currents are often applied in the channel to enhance the performance of high speed devices, and consequently Joule self-heating occurs. Although graphene has extremely good thermal conductivity [3], the overall heat dissipation of graphene device is controlled by the thermal resistance of the system, which depends on the device structure, interface resistance, substrate material, etc. Understanding the heat spreading of graphene devices is important because self-heating effects can limit the effective carrier mobility of the graphene [4, 5], maximum current carrying capability [6], and overall device reliability. In this study, we conducted a three dimensional (3-D) thermal simulation to investigate the heat dissipation characteristics of the device structure. Pulsed and DC current of graphene resistor were also measured under various temperature and bias conditions.

A physically-based device simulator (Sentaurus TCAD of Synopsys) was used for the 3-D simulation, with reported parameters for graphene-substrate interface thermal resistance [7]. The baseline structure is a non-gated epitaxial graphene device [1] which has source-to-drain length (L_{SD}) of 500 nm, graphene channel width of 6 um. A 300 K heat sink is located at the bottom of the SiC substrate, which is a very good thermal conductor. A large volume outside of the device region was included to allow for 3D heat spreading. Figure 1(a) shows a representative simulation structure with lattice temperature distribution for uniform DC power dissipation over the channel area. A zoom-in image (b) and a cut-area (c) indicate better cooling near the metal contact and the edge of the graphene. The relation of input power density (P_{in}) and the junction temperature (T_{Max}) is shown in Figure 2 (a) for several graphene-substrate interface resistance (R_{int}) values. T_{Max} is 380 K for P_{in} of $2\cdot10^6$ W/cm^2, when $R_{int}=8.8\cdot10^{-9}$ K m^{2}W^{-1} [7]. R_{int} is an important factor in the simulation results, since the majority of the heat spreads into the substrate while only a small amount of heat is relieved by source and drain contacts, even for short channel lengths; the lateral heat diffusion component along the graphene layer is ~14% out of total power input for L_{SD}=100nm and only ~1% for L_{SD}=500nm. T_{Max} vs. L_{SD} relation is described in Fig. 2 (b) and (c), for uniform P_{in} over the channel and 50nm width fixed area local heating, respectively. The limited relief to the hotspot in the middle of the channel is reduced even more with longer L_{SD}.

Pulsed and DC currents vs voltage were measured for two-terminal non-gated epitaxial graphene devices over the temperature range of 225K~375K. The pulse time is 200 ns with 1ms spacing. The temperature dependence of pulsed current I_D was found to follow $I_D(T+\Delta T) = I_D(T)\cdot(1-\alpha\cdot\Delta T)$ (Fig. 3 (a)), and the extracted α is 0.0019 /K for V_D of 2.5V. The I_D change vs. temperature is expected to be a combined effect of mobility degradation and carrier generation with increasing temperature. Figs. 3 (b) and (c) show that a shorter pulse time results in higher current as a result of lower self-heating. Self-heating is not eliminated completely, however, since 200 ns was the shortest pulse length we could apply, while reported time constants are in 30~300 ns range [5], and heating time-dependence is not exponential. The simulation showed a very rapid heating until 20 ns then slower temperature increase with constant power level. The rise time of the pulse also affects the heating profile. The difference in measured currents for pulses of duration 2μs and 200ns can be used together with the data of Fig. 3(a) to estimate that for a representative input power of P_{in}=20mW/μm^2, the temperature difference ($T_{2\mu s}$-T_{200ns}) produced by self-heating is 55ºC (corresponding to ($T_{2\mu s}$-T_{200ns}) /P_{in} = $2.75\cdot10^{-9}$ Km^{2}W^{-1}). The absolute T_{Max} value vs. P_{in} is hard to estimate from the measurement because of possible self heating from 200 ns pulses. If the entire nonlinearity of the I_D-V_D curve is assumed to be the result of heating, T_{2us} can be estimated to be 161ºC for P_{in}= 20mW/μm^2, in substantial agreement with fig. 2(b).

In summary, self-heating of graphene rf devices is inevitable due to their small time constants and the need for driving high currents in the channel. A high quality graphene-substrate interface with high

thermal conductivity substrate is important for lower thermal resistances. Shorter channel length is also favorable to utilize lateral heat spreading.

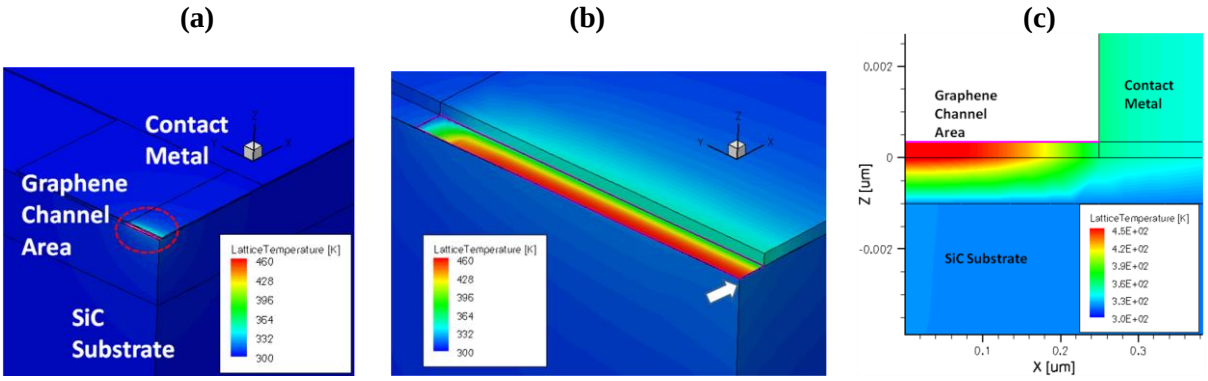

Fig. 1 (a) 3-D simulated lattice temperature of graphene resistor. A quarter of the device is shown here. (b) Zoom-in figure of (a) which shows cooling effect from the metal contact and side edge of the channel. Hottest point is indicated by white arrow. (c) Cut-area at the middle of the channel.

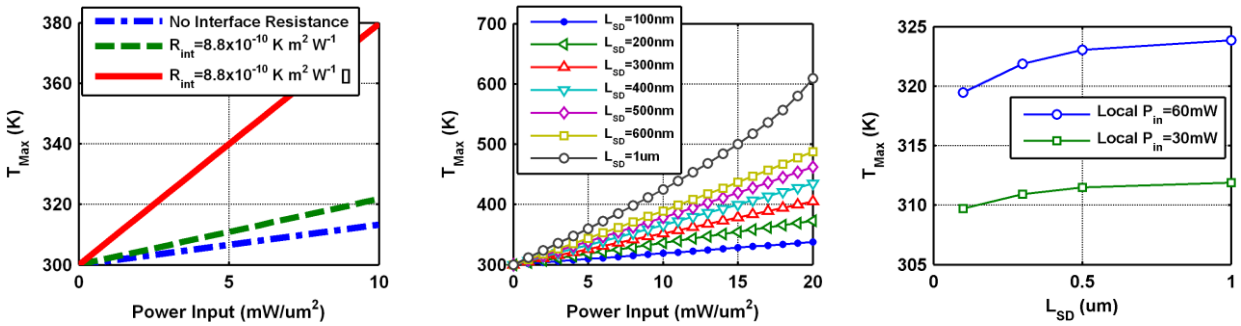

Fig.2 (a) Simulated junction temperature (T_{Max}) with graphene-substrate interface resistance variation. (b) Simulated T_{Max} for various L_{SD}. Power input density is uniform for all cases. (c) Simulated T_{Max} for various L_{SD}, when local heating is applied to a 50nm width strip in the middle of the channel.

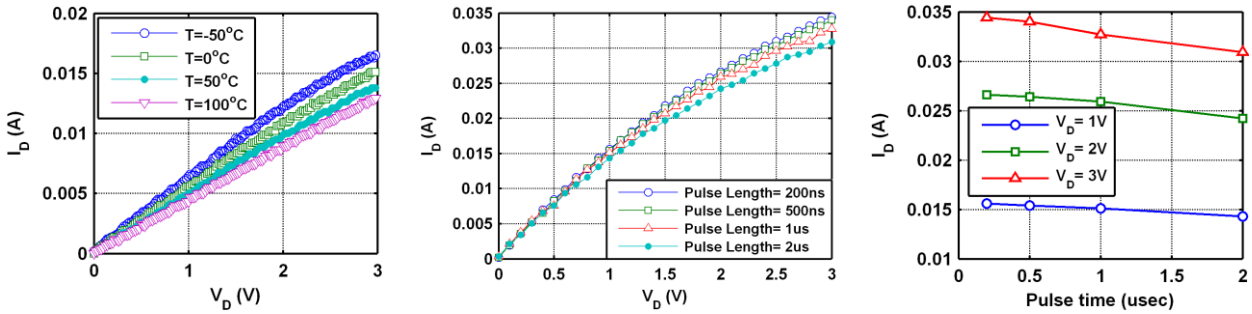

Fig. 3 (a) Measured pulse I-V under various temperatures. Higher temperature gives lower current level. (b) Measured pulse I-V with pulse time variation. Increment of current due to less heating is shown when the pulse time is reduced. (c) I_D vs. pulse time for various V_D.

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