Student Paper

Redox-Active Molecular FLASH Memory to Replace SRAM

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The dimensional scaling of microelectronics to improve CPU performance is facing fundamental challenges. One current strategy is to increase the cache memory – static random access memory – which, unfortunately, can decrease CPU net information throughput because it is volatile and occupies a large chip space. Floating-gate non-volatile memory (NVM) is compatible with CMOS integration. However, the conventional charge-storage mediums operate at large Program/Erase (P/E) voltage and endure only 10^5 P/E cycles. Redox-active molecules have been recently considered as attractive floating gate materials for charge storage. Redox molecules can be engineered to attach on Si structures with simple and low-cost processes, retain robust states, and endure more than 10^{12} P/E cycles. [1] Due to the inherent oxidation and reduction of the redox centers, molecules can exhibit distinct charged or discharged states which can represent logic ON and OFF states with fast P/E speed and excellent endurance.

In this work, we have integrated redox-active molecules (α-Ferrocenylethanol) into a Si-based platform for molecular flash memory. Molecular attachment on Si and SiO_2 were characterized by cyclic voltammetry (CyV) and X-ray photoelectron spectroscopy (XPS). The CyV curves demonstrated oxidation (reduction) peaks at negative (positive) gate voltage. The XPS results indicate the molecule successfully attaches on both SiO_2 and Si surfaces, and that the molecule survives the atomic layer deposition of Al_2O_3. A large memory window was obtained on metal-Al_2O_3-ferrocene-Si (MAFOS) capacitors. Poor erase speeds in the metal-Al_2O_3-ferrocene-Si (MAFS) devices during P/E operations indicate that it is more difficult for the molecules directly attached on Si to stay positively charged without an isolation layer. Fig. 4c and 4d shows the endurance characteristics. The MAFS devices fail after 10^7 P/E cycles, while the MAFOS devices still behave well even after 10^9 P/E cycles. The slight up-shift observed is due to the accumulation of electrons in deep traps and can be resolved by selecting proper P/E voltages. [2]

Based on the above results, we integrated the MAFOS structure as the gate stack on Si-nanowire (SiNW) FETs to study molecular-based flash memory with a truly nanoscale channel. Counterclockwise hysteresis loops were observed in I_{DS}-V_{GS} curves, indicating the charge storage mechanism. A nearly cutoff state was observed, and the On/Off ratio is as high as ~10^7. No memory window is observed for reference samples without molecules evidence that charge storage in the Al_2O_3 is negligible. The erase speed is faster than program speed. This imbalance is because the energy for electrons to be injected into the ferrocene lowest unoccupied molecular orbital (LUMO) (2.28 eV) is much higher than that for holes to be injected into the highest occupied molecular orbital (HOMO) (0.59 eV). A similar staircase behavior was also obtained (Fig. 7b). Excellent endurance property was obtained. Negligible memory window degradation was observed after 10^9 P/E cycles by using 100 μs gate voltages. With 500 μs P/E voltages, the devices are well functional after 10^8 P/E cycles.

In summary, we have shown that the integration of redox-active molecules in a solid-state Si-based platform can generate high-performance molecular flash memory which will enable a vast opportunity for on-chip and local memory.

References

[1] Z. Liu, A. A. Yasseri, J. S. Lindsey, and D. F. Bocian, "Molecular memories that survive silicon device processing and real-world operation," *Science*, vol. 302, pp. 1543-1545, Nov. 2003.

[2] Y. Wang, W. S. Hwang, G. Zhang, G. Samudra, Y. C. Yeo, W. J. Yoo, "Electrical characteristics of memory devices with a high-*k* HfO_2 trapping layer and dual SiO_2/Si_3N_4 tunneling layer," *IEEE Trans. Electron Dev.*, vol. 54, no. 10, pp. 2699-2705, Oct. 2007.

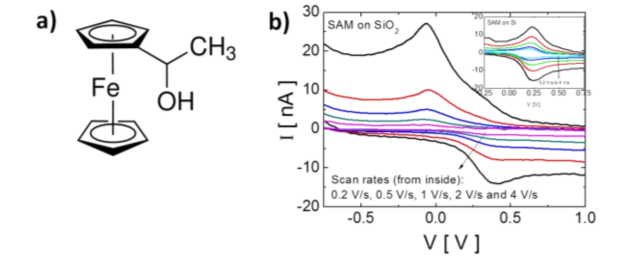

Fig. 1 (a) α-Ferrocenylethanol molecular structure; (b) CyV of electrolyte-ferrocene-SiO_2-Si capacitor; Inset: CyV of electrolyte-ferrocene-Si capacitor. The surface coverage of SAM calculated from the oxidation peaks were 5.23×10^{13} cm^{-2} and 3.14×10^{13} cm^{-2} on Si and SiO_2 surface, respectively.

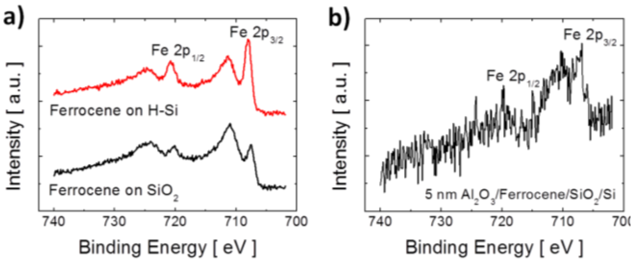

Fig. 2 (a) and (b) XPS of SAM on Si and SiO_2 before and after deposition of Al_2O_3.

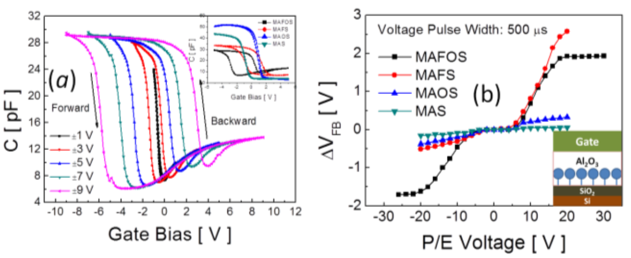

Fig. 3 (a) capacitance-voltage hysteresis curves of the MAFOS device. Inset: Hysteresis with gate voltage sweep ranges of ±5 V of MAFOS and control samples; (b) ΔV_{FB} as a function of P/E voltage. Inset: schematic of MAFOS capacitor memory cell. The charge density in the SAM of MAFOS device at this P/E condition was calculated as 4.82×10^{12} cm^{-2}.

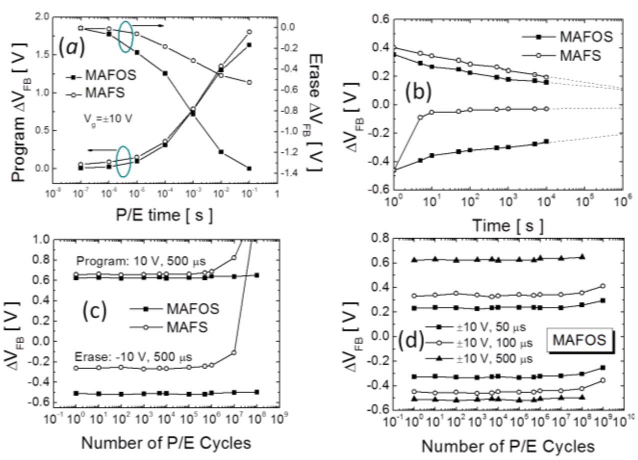

Fig. 4 (a) P/E speed (b) retention (c) endurance characterizations of MAFOS and MAFS devices; (d) excellent endurance of MAFOS under P/E voltage = ±10 V with shorter V_G pulses.

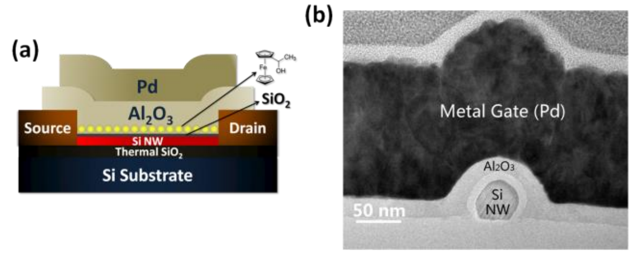

Fig. 5 (a) Schematic structure of molecular memory with MAFOS stack as the gate stack on SiNW FETs; (b) TEM image of the cross-section of a such molecular memory.

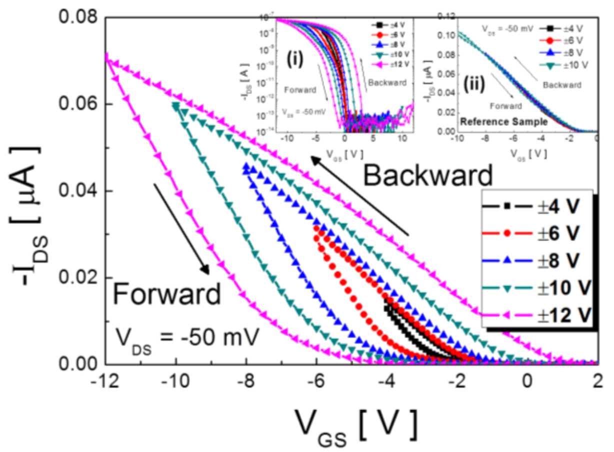

Fig. 6 The charge storage in the embedded SAM induced large memory window. Inset: (i) transfer characteristics of MAFOS molecular memory cell with counterclockwise hysteresis loops; (ii) I_{DS}-V_{GS} curves of a reference sample without SAM showing negligible memory window.

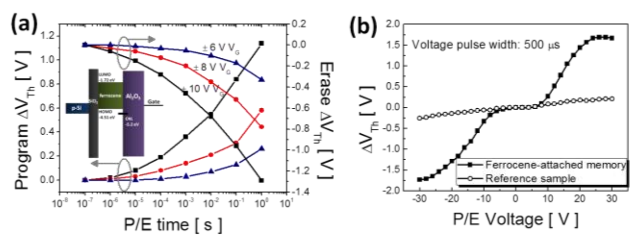

Fig. 7 (a) P/E speed characterizations of MAFOS devices under different gate voltages. Inset: schematic band diagram of the p-Si/SiO_2/ferrocene/Al_2O_3/gate system; (b) ΔV_{Th} of MAFOS and reference sample as a function of P/E voltage. The charge density of the SAM in MAFOS device is around 6.96×10^{12} cm^{-2}.

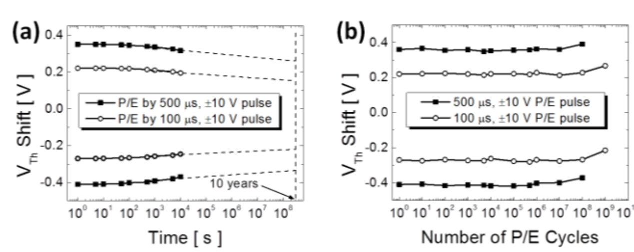

Fig. 8 The molecular FLASH cells exhibit excellent (a) retention and (b) P/E endurance (> 10^9 cycles).