Student Paper

A Variational Thermodynamic Approach for Modeling Capacitance of a Single-gated MOS Device with Multiple Interacting p-Si and n-Si Components

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Here we develop and apply a Variational Thermodynamic (VT) methodology to produce a comprehensive theory of the capacitance – voltage (C-V) characteristics of a single-gated multi-component device. Our approach consists of minimizing the Helmholtz Free Energy (F) [1] of the device by expressing F in terms of the internal electrical potentials which develop in response to the application of external sources at its terminals [2-3]. Our VT approach avoids complications in Finite Element (FE) analysis due to the highly non-linear source term given by mobile charge generation. Another attractive aspect of our method is that edge effects, internal discontinuities, fringe fields, etc., are easily handled using perturbation methods.

In order to exercise our methodology, we have applied it to a real Trench Insulated Gate Bipolar Transistor (TIGBT), the cross-section of which is shown in Fig.1. Figure 2 presents the entire VT methodology flow for the device. First, we evaluate F using charge statistics and potential trial functions $\hat{\phi}$ shown in Fig. 3 for each active region of the device. Next, we determine the relaxation distances ('w's) of the potential as a function of the interface potentials ('ϕ_S's) shown in Fig. 4. Then, the 'ϕ_S's are determined as functions of the gate voltage, V_G shown in Fig. 5 [4]. Our model accommodates either Boltzmann or Fermi-Dirac statistics for mobile charges. The series combination of the oxide and individual junction capacitances for the P-base and N^- -drift region predicted by our model are shown in Fig. 6. Finally, the model C_{GE} is constructed by adding these series combinations in parallel. We have measured a real TIGBT, IXGH50N0B4, using Keithley Model 4200 Semiconductor Characterization System. In Fig. 7, we compare our model C_{GE} with the measured gate-to-emitter C-V characteristics. Our model matches well with the experiment. Figure 8 consists plots of i) gate potential, V_G vs. interface potential, ϕ_{SP} (open triangle) and ii) relaxation distance, w_{sp} vs. ϕ_{SP} (open circle) for P-base region. These overlaid plots are used to determine the threshold voltage (V_{th}) of the device to be 4V, which is within the range of V_{th} specified in the device datasheet [www.ixys.com].

In this paper, we have proposed and developed a novel physics-based methodology to treat the electrostatic behavior of a multi-region silicon device in which mobile charges are significantly – even dominantly – present. Our model shows that mobile charges, acting as entropy, consume energy from the gate without changing the state of the device. This verifies that the TIGBT is indeed an entropy-producing heat engine. An attractive application of our VT methodology would be in the area of modeling semiconductor device characteristics to predict their behavior with sufficient fidelity to justify delaying commitment to silicon and further the total development process in terms of optimizing dimensions, doping levels, etc. We believe that our model has sufficient conciseness that it can play a useful role in automated design optimization schemes leading toward development of future generation TIGBTs.

References:

[1] D. Landau, E.M. Lifshitz, and L.P. Pitaevskii, "Electrodynamics of Continuous Media", Butterworth-Heinemann, Burlington, MA, 2008, p.19. [2] N.G. Gunther, A. A. Mutlu, and M. Rahman, "Quantum-mechanically corrected variational principle for metal-oxide semi-conductor devices leading to a deep sub-0.1 micron capacitor model," *Journal of Applied Physics*, vol. 95, pp. 2063 – 2072, Feb. 2004. [3] A. Sattar, N. Gunther,and M. Rahman. "Modeling the Capacitance-Voltage Characteristics of the Trench Insulated Gate Bipolar Transistor (TIGBT) by Minimizing its Helmholtz Free Energy," in I.S.D.R.S. 2011, FA8-02, 2011. [4] L. Boyer, O.Fruchier, P. Notingher, S. Agnel, A. Toureille, B. Rousset and J. Sanchez, "Analysis of Data Obtained Using the Thermal-Step Method on a MOS Structure—An Electrostatic Approach", *IEEE Trans. Of Industry Applications*, vol.46, no.3, pp.1144-1150, Fig. 10-11, May, 2010.

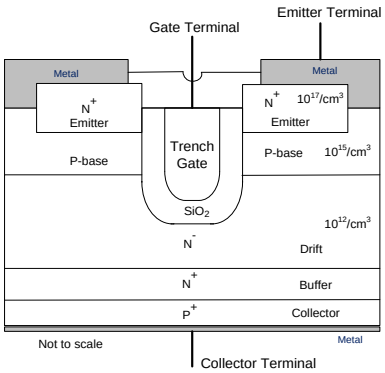

Figure 1: The cross section of a 600V Trench-Gated IGBT structure.

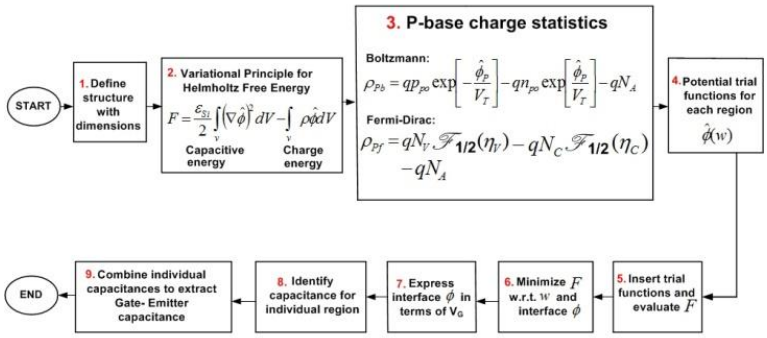

Figure 2: VT Methodology flow for obtaining MOS capacitances.

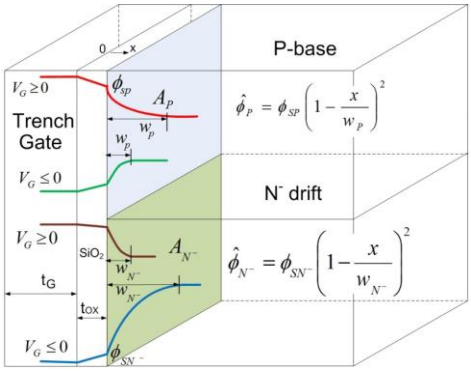

Figure 3: Potential trial functions in P-base, N^--drift regions, oxide and trench gate.

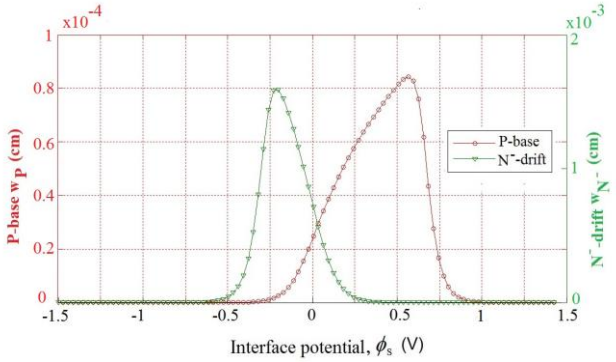

Figure 4: Relaxation distance, w vs. Interface potential ϕ_S for P-base (red) and N^--drift (green) regions.

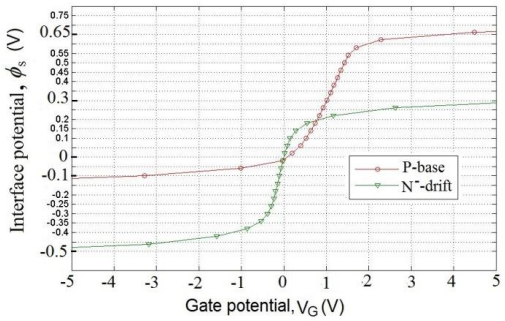

Figure 5: Interface potential, ϕ_S vs. gate potential V_G for P-base (red), and N^--drift (green) regions.

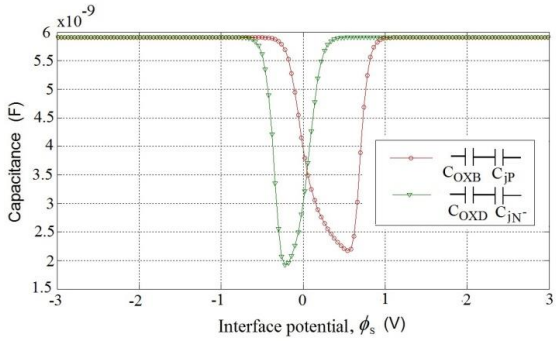

Figure 6: Junction capacitance, C_j in series with oxide capacitance vs. interface potential, for P-base (red) and N^--drift (green) regions.

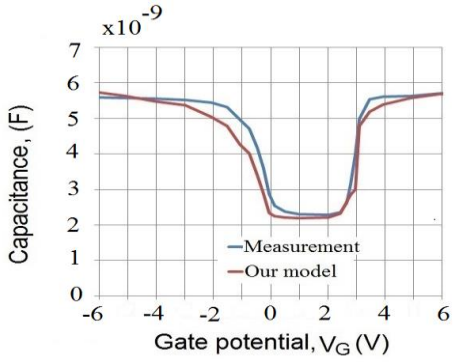

Figure 7: Measured gate-to-emitter capacitance (blue) and our model (red).

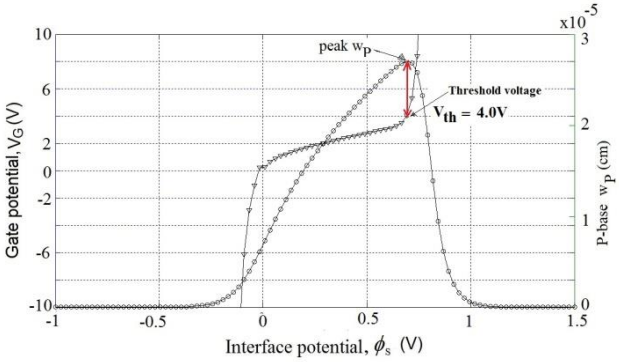

Figure 8: Determination of TIGBT threshold voltage, V_{th} using the overlaid plots of i) gate potential, V_G vs. P-base interface potential, ϕ_{SP} from Fig. 5 and ii) P-base w_p vs. interface potential, ϕ_{SP} from Fig. 4.