Student Paper

Stability Criteria of LC Oscillators in nanoscale DG-MOSFETs

Soumyasanta Laha and Savas Kaya

School of Electrical Engineering and Computer Science, Ohio University, Athens, OH 45701, USA,
{sl922608, kaya}@ohio.edu

The stability criterion of the widely popular negative resistance LC oscillator for sustained oscillations built with nanoscale Double Gate MOSFETs (DG-MOSFET) is presented. The stability criterion of $g_m R \geq \frac{1}{2}$ is modeled by a small signal quantitative analysis. This is a less stringent oscillatory criterion compared to an equivalent oscillator, designed in conventional CMOS. The design and simulation are implemented in 32 nm FinFET technology.

The DG-MOSFET is simple for 3D structural optimization and relatively easier to fabricate among the different multi-gate MOSFET structures (MIGFET, π-MOSFET and so on). Therefore, the DG-MOSFET (Fig. 1a) based on a modified (two gates separated and independently accessed) FinFET device architecture is chosen for our analysis in this paper. This multi-gate nano structure [1]-[3] can efficiently control the channel from two sides of the channel instead of one side as in planar bulk MOSFETs. The ability to alter channel potential by two gates provides a relatively easier and sturdy way to control the channel electrostatics, reducing the short channel effects and leakage concerns considerably. The device works in two different modes, the common mode, when the gates are joined and independent mode, when the gates are separated. The $I_D - V_{fg}$ characteristics of these two modes of such a device are observed in Fig. 1b. The capacity to handle GHz modulation [4] and independent gate-drive mode make the DG-MOSFET an ideal choice also for tunable analog/mixed signal RF applications. Here we expand this trend by exploring the LC oscillator in common mode DG-MOSFET via quantitative analysis and computer simulations.

As we know a simple LC resonance circuit ceases to oscillate primarily due to imperfectness of the inductor, L which gives rise to resistive losses, that determines the quality factor, Q of the inductor/LC tank. The resistive loss, R_p is eliminated by the design of a latch circuit that essentially acts as a negative resistance to nullify the effect of positive resistance of the lossy tank. The condition to oscillate for the single gate CMOS based LC oscillator is given by [5]

$$g_m R_p \geq 1 \quad \ldots (1)$$

We analyze the DG-MOSFET small signal oscillator circuit (Fig. 2) to verify that the criterion for oscillation of the negative resistance common mode LC oscillator is less stringent than that of its single gate CMOS counterpart. To start with the analysis, we design an equivalent differential circuit of the LC oscillator and focus on transistor MN_2 as depicted in the figure. The current, I, determined from the analysis is given by

$$I = \frac{\frac{V}{2}}{r_{dsf}+r_{dsb}} - \frac{(g_{mf}+g_{mb})}{2} \quad \ldots (2)$$

The DG-MOSFET considered here operates in common mode configuration (two gates are joined) and therefore we can safely assume $g_{mf} = g_{mb} = g_m$ and $r_{dsf} = r_{dsb} = r_{ds}$. Therefore, the current is modeled as,

$$I = \frac{V}{4r_{ds}} - g_m V \quad \ldots (3)$$

Ignoring r_{ds}, since typically $g_m \gg \frac{1}{r_{ds}}$ in today's transistor, we have,

$$I = -g_m V \quad \ldots (4)$$

The input resistance of the oscillator (loss of the tank), $2R_p = \frac{V}{I}$ (Fig. 2) is given by,

$$2R_p = -\frac{1}{g_m} \quad \ldots (5)$$

To sustain oscillation, the negative resistance must cancel the loss of the tank [5]. Therefore,

$$2R_p \geq \frac{1}{g_m} \quad \ldots (6)$$

Rearranging,

$$g_m R_p \geq \frac{1}{2} \quad \ldots (7)$$

Comparing Eqns. (1) and (7) it becomes obvious that the criterion for oscillation of a DG-MOSFET LC oscillator is more lenient than conventional CMOS. The better leniency implies the inductor Q can afford to be inferior to sustain the oscillation. The output waveform of the common mode DG-MOSFET at 60 GHz is observed form Fig. 3. It is to be noted that since the combined g_m (of two gates) of DG-MOSFET is much higher than the g_m of conventional CMOS [7] it can be safely assumed that the g_m of a single gate of a DG-MOSFET is approximately equal/comparable to the g_m of a conventional CMOS.

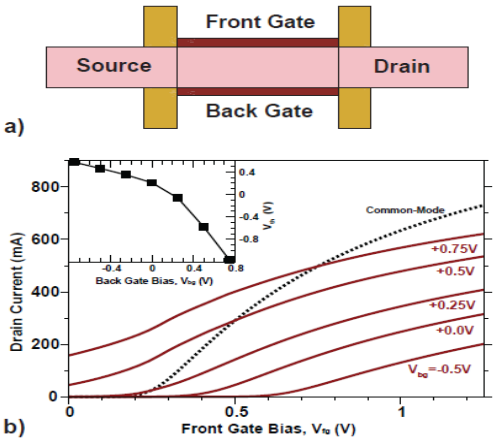

Fig. 1. a) The generic DG-MOSFET device structure. $I_D - V_{fg}$ characteristics of an n-type Independent and Common Mode DG ($V_{fg} = V_{bg}$) transistors. The inset shows the resulting shift in the front gate threshold.

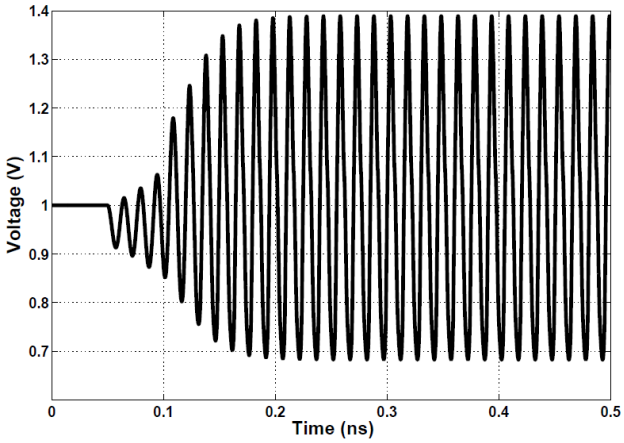

Fig 3. The output waveform of the common mode DG-MOSFET at 60 GHz. The simulation is performed in ASU-PTM 32 nm FinFET [5] technology using Synopsys HSPICE RF.

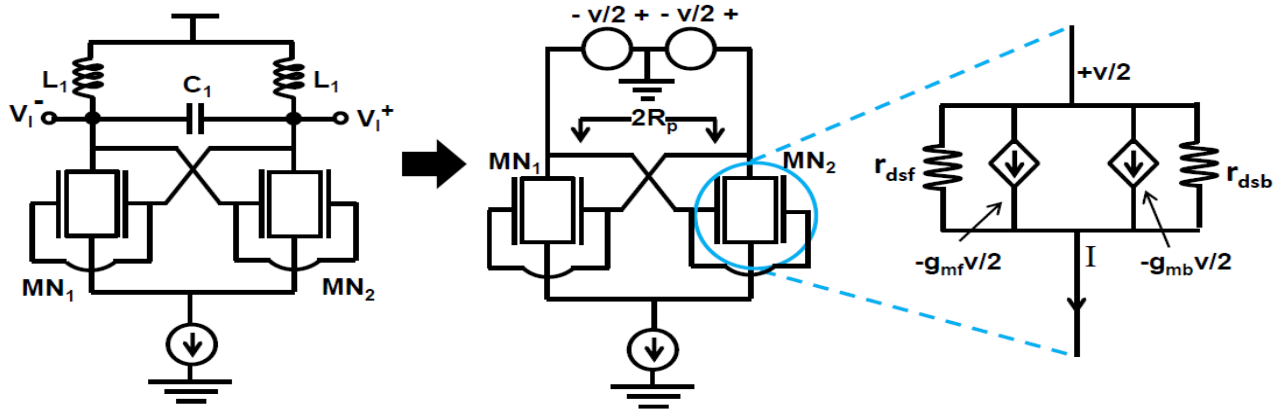

Fig. 2. The negative resistance LC oscillator in common mode DG-MOSFET. At resonance, the LC tank becomes resistive only and the latch circuit acts as negative resistance to nullify its effect. The small signal analysis of a DG-MOSFET is focused to study the criterion for oscillation.

References:

[1] T. Skotnicki, J. A. Hutchby, T.-J. King, H.-S. Wong, and F. Boeuf, "The end of CMOS scaling," IEEE Circuits Devices Mag., pp. 16–26, 2005.
[2] K. Ahmed and K. Schuegraf, "Transistor Wars," IEEE Spectr., p. 50, Nov 2011.
[3] I. Ferain, C. A. Colinge, and J.-P. Colinge, "Multigate transistors as the future of classical metal oxide semiconductor field-effect transistors," Nature, vol. 479, pp. 310–316, Nov 2011.
[4] A. Lazaro and B. Iniguez, "RF and Noise performance of Double Gate and Single Gate SOI," Solid State Electronics, vol. 50, pp. 826–842, 2006.
[5] B. Razavi, RF Microelectronics. Boston, USA: Prentice Hall, 2012.
[6] W. Zhao and Y. Cao, "Predictive Technology Model for Nano-CMOS Design Exploration," ACM Journal on Emerging Technologies in Computing Systems, vol. 3, pp. 1–17, 2007.
[7] J.-P. Raskin, et. al."Analog/RF Performance of Multiple Gate SOI Devices: Wideband Simulations and Characterization," IEEE Trans. Electron Devices, vol. 53, pp. 1088–1095, May 2006