Student Paper

Electrical Characteristics of Atomic Layer Deposited High-k Dielectrics on InN

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InN is a promising channel material for THz electronics due to its low electron effective mass [1]. Low interface state density and low leakage dielectrics on InN are essential for device applications. Here, we first report on the electrical characteristics of atomic layer deposited (ALD) deposited high-k dielectrics on InN.

Since the discovery of lower bandgap of InN in materials grown by MBE, the electron velocities have been predicted to be very high (> 5×10^7 cm/sec) [2]. Experimental data also suggest the high electron velocity potential of InN. These properties make it an ideal candidate for high frequency electronic devices. However, a deep conduction band pinning [3] of the InN surface has been a formidable challenge to practical device applications. Various *in-situ* and *ex-situ* surface cleaning methods have been reported with partial unpinning of the surface [4~8]. However, there has not been any report on dielectric/InN interfaces. Here, we first report on the capacitance-voltage characteristics of ALD deposited dielectrics on InN. Recently ALD dielectrics have been highly successful in realizing low interface state dielectrics on III-V and GaN [4] due to its low damage process and its flexibility in the growth rate, initial bonding configuration. Dielectric deposition on InN by ALD is a promising process.

The layer structure of the InN MOSCAP wafers is shown in Fig.1 (a). The In-polar device was grown by plasma-assisted molecular beam epitaxy (PA-MBE) on sapphire substrate with a 1 μm thick GaN buffer layer. A thin top InGaN layer was grown to have a lower surface pinning. Fig.2 shows scanning electron microscope (SEM) image and atomic force microscope (AFM) image of InN with and without oxide. Both SEM and AFM show a rough surface and oxide layer follows InN surface completely. ALD dielectrics were deposited with *ex-situ* surface treatments. Hydrochloric acid [5, 6] and ammonia sulfide [7, 8] have been reported to reduce surface electron accumulation and alleviate downward band bending. One wafer was treated by hydrochloric acid (HCl) (~15%) at 50 ºC for 10 min and the other one was treated by both hydrochloric acid (~15%) at 50 ºC for 10 min followed by ammonia sulfide ($(NH_4)_2S$) (~44%) at 50 ºC for 45min. The wafers were then immediately loaded into the ALD chamber. A composite Al_2O_3/HfO_2 gate dielectric of 14 nm/ 2 nm and 10 nm /10 nm thickness were deposited on the HCl treated and $(NH_4)_2S$ treated samples respectively. The Al_2O_3 layer was deposited at 300 ºC and the HfO_2 layer was deposited at 150 ºC. Next, Ni/Au gate contacts were patterned, followed by BCl_3/Ar RIE to form mesas. Ti/Au was used for the bottom ohmic contacts. The top-view of a finished devices is shown in Fig.1 (b), by following the process flow in Fig.3.

Current-voltage and capacitance-voltage curves were measured using Agilent semiconductor parameter and impedance analyzer respectively. The I-V results in Fig.4 show that the thicker oxide layer provides smaller current leakage. Both samples show good insulating dielectrics with low leakage. The C-V curves at different frequencies in Figs 5 (a) and (b) show the same trend for both samples, they do not show any bulk electron depletion and with increasing of frequency, capacitances decrease. A SILVACO ATLAS simulation (Fig. 6 (a) and (b)) of the structures suggests high interface state densities (~ 3×10^{13} cm^{-2}) inside the conduction band.

In conclusion, we report on the electrical properties of ALD deposited dielectrics on InN. Post deposition annealing treatments in forming gas will be investigated to reduce the observed high interface state density.

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References

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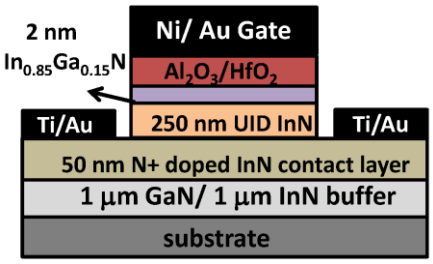
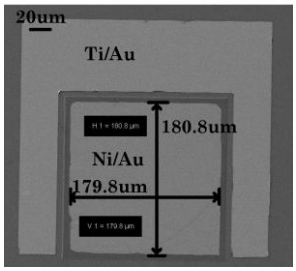
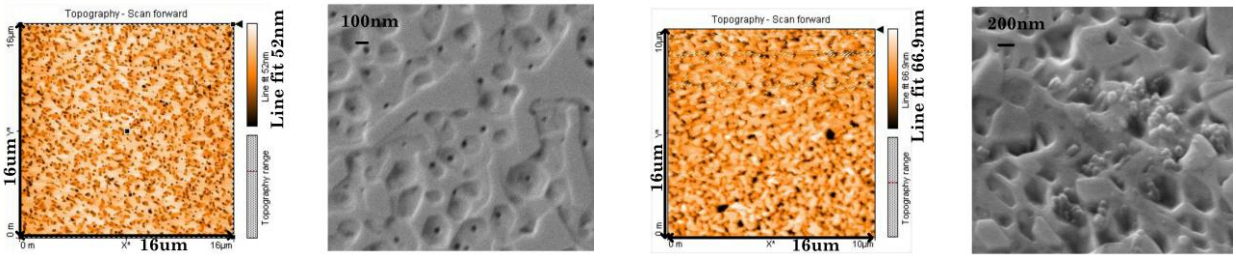


(a) Cross-section schematic of InN MOSCAP



(b) SEM top view of finished InN device

Fig.1 (a) InN MOSCAP device structure, (b) SEM top view of finished device



(a) (b) (c) (d)

Fig.2 AFM (a) and SEM (b) of InN surface; AFM (c) and SEM (d) of oxide surface on InN

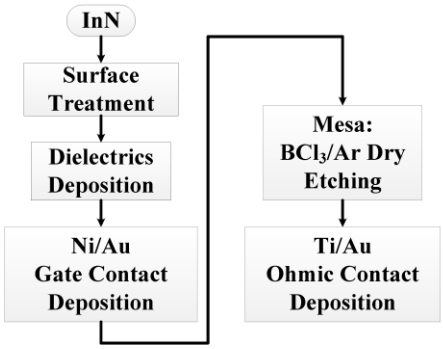


Fig.3 Process flow

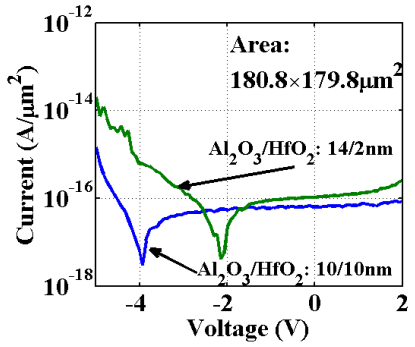
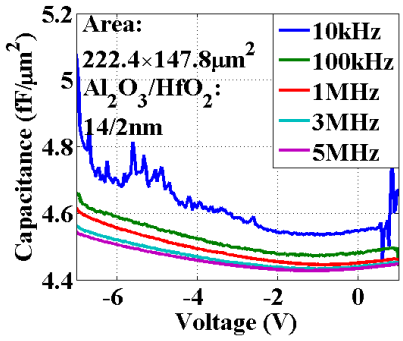
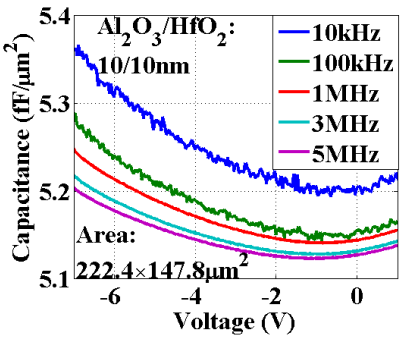


Fig.4 I-V curves of MOSCAPs InN

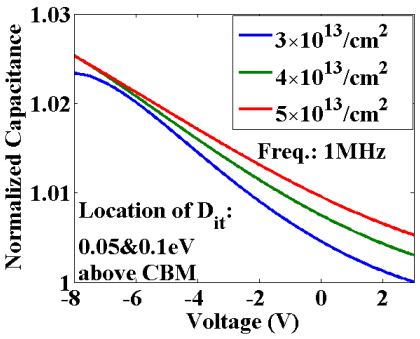


(a)

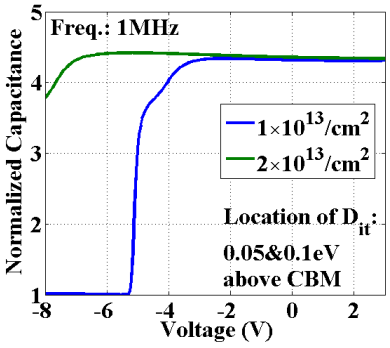


(b)

Fig.5 Frequency dependent C-V of MOSCAPs, (a) HCl treated sample, (b) HCl and $(NH_4)_2S$ treated sample



(a)



(b)

Fig.6 Devices simulation on interface trap density in SILVACO ATLAS: high D_{it}, (b) and low D_{it}