Student Paper

Embedded Germanium PIN Photodetectors in ALD Slot Waveguides

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SOI Silicon photonics technology is becoming mature for on-chip photonic integrated circuits (PIC). SOI photonic chips and high performance components are standardized and produced in foundries [1]. Low loss and compact crystalline silicon waveguide technologies have been demonstrated using the high refractive index contrast and ultra-low absorption in the C-band range. However, SOI wafers are costly and integration of the SOI waveguide technology with the standard CMOS transistor technology faces problems. A modern fully depleted SOI (FDSOI) wafer, manufactured for the 14nm transistor technology with a device layer of 12nm and the buried oxide (BOX) layer of 25nm[2] is not suitable for photonics applications. Industrial requirements for 3D integration and multilevel interconnection architecture in CPUs demand a more flexible technology than the conventional SOI. Back-end deposited waveguide technology is a more flexible solution and deposited polysilicon waveguides, ring resonators, modulators have been demonstrated by Ho et. al.[3].

In this paper, integration of slot waveguides with embedded photodetectors is investigated. The schematic of architecture is shown in Fig.1. Fabrication of the waveguides and grating couplers is explained elsewhere [4, 5]. The waveguide-detector integration is depicted in Fig. 2. The coupling of the optical mode is demonstrated using finite element simulations. It is deduced that due to refractive index contrast a fraction of the light is back reflected. Sidewall angle and roughness caused by etching will dramatically decrease the back reflection of the guided mode.

The Ge photodetector is a PIN diode and the light is detected in the intrinsic region. Diode mesas are formed using selective Ge epitaxy using reduced pressure chemical vapor deposition (RPCVD) technique. All germanium layers are grown using digermane as Ge precursor where HCl was introduced to ensure the selectivity of the growth. At first a germanium layer is grown at 400°C. The purpose of this layer is to terminate the defects in germanium due to high lattice mismatch with silicon. Defect-free germanium is sequentially grown at 670°C on the buffer later. The total thickness of Ge PIN was 1.8μm as shown in Fig. 2a. A more illustrative picture of the Ge stack grown on silicon is shown in Fig. 2b where the oxide is stripped. The layers were in-situ doped with boron and phosphorous to form p- and n-type germanium, respectively. The growth rate of PIN mesa was dependent on pattern layout and the deposition rate is higher in smaller area openings. As a result, the dopant concentration may be varied over different opening sizes as well.

The photodetectors were electro-optically characterized. Generated photocurrent was measured using a fiber C-band tunable laser source. The measurements were performed at 1.2V and 1.7V bias voltage respectively and the intensity of the laser was swept from zero to 4mW. The incident light was vertical to the wafer plane. The results are demonstrated in Fig 4(a). Furthermore with a bias voltage kept at 1.2V the incident light wavelength is swept from 1525nm to 1575nm to measure the sensitivity of the detector. Fig. 4(b) shows the photocurrent response versus wavelength. Several square shape opening areas were characterized and the lowest dark current was seen in the smallest opening area ($50 \times 50\mu m^2$). These results are summarized in Fig. 4(c).

Presented results demonstrate that the selective growth technique has the potential to deposit the detector structure directly on Si where they can be easily integrated with other components e.g. modulators or lasers in 3D photonic integrated circuits. As a result a multi layered interconnection system can be achieved at the back end of modern CPU cores.

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[1] ePIXfab. IMEC standard silicon photonics [Online] http://www.epixfab.eu/.
[2] Shin-Etsu Chemical Co.Workshop on FDSOI 14nm technology [Online] http://www.soiconsortium.org/fully-depleted-soi/presentations/june-2013/Nobuhiko%20Noto%20-%20UTBB%20Wafer_SEH_June2013.pdf
[3] Y. H. D. Lee and M. Lipson, *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 19, no. 2, pp. 409–415, Mar. 2013.
[4] M. M. Naiini, C. Henkel, G. B. Malm, and M. Ostling, *71th Device Research Conference*, 2013.
[5] M. M. Naiini, C. Henkel, G. B. Malm, and M. Östling, *Solid-State Electronics*, vol. 74, pp. 58–63, Aug. 2012.

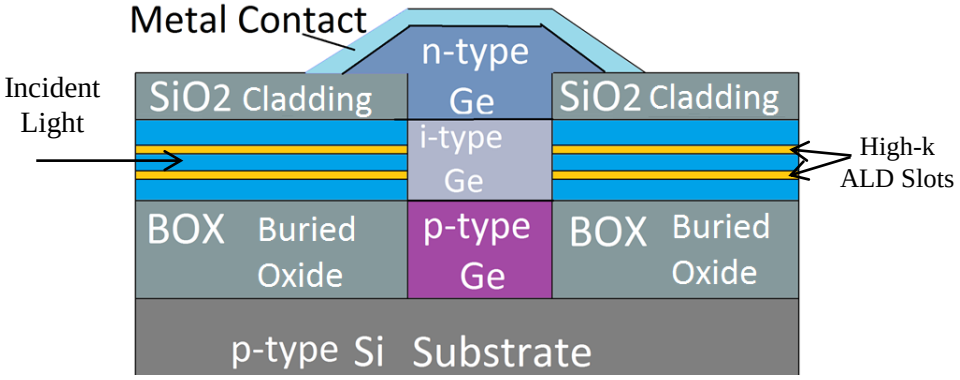

Fig.1. Schematics of the waveguide-detector junction. The detector mesa is grown after fabrication of the waveguides. A PIN diode is formed using epitaxy. The incident light will face the intrinsic germanium to maximize the quantum efficiency.

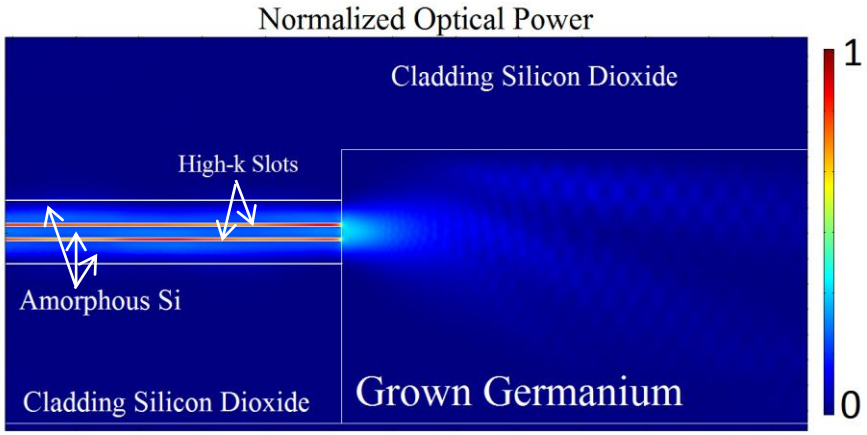

Fig.2. Simulated wave propagation profile representing the normalized optical power. Coupling of the guided mode into the germanium active region is demonstrated. High optical mode confinement can also be observed in the slot regions. The circuit is designed for the TM mode.

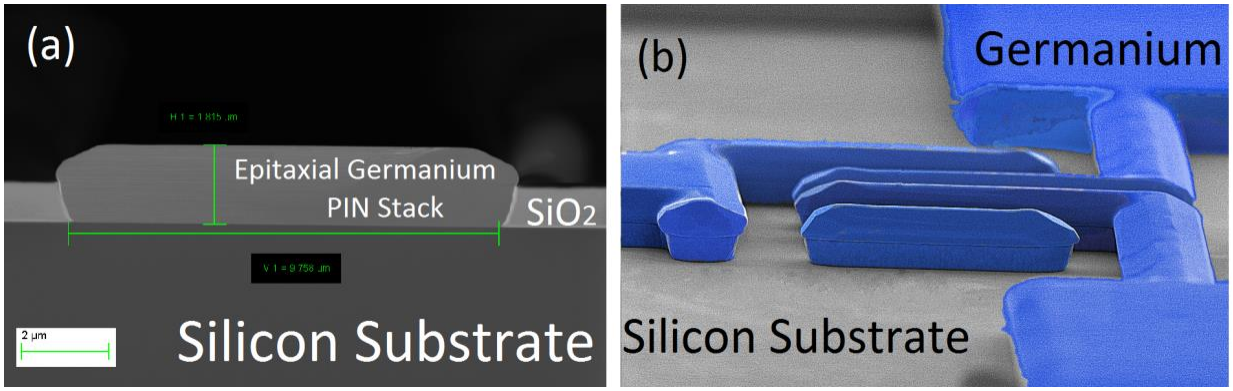

Fig.3. (a) Cross section SEM micrograph of the selectively grown PIN junction. (b) SEM image of grown germanium extruded features using selective epitaxy.

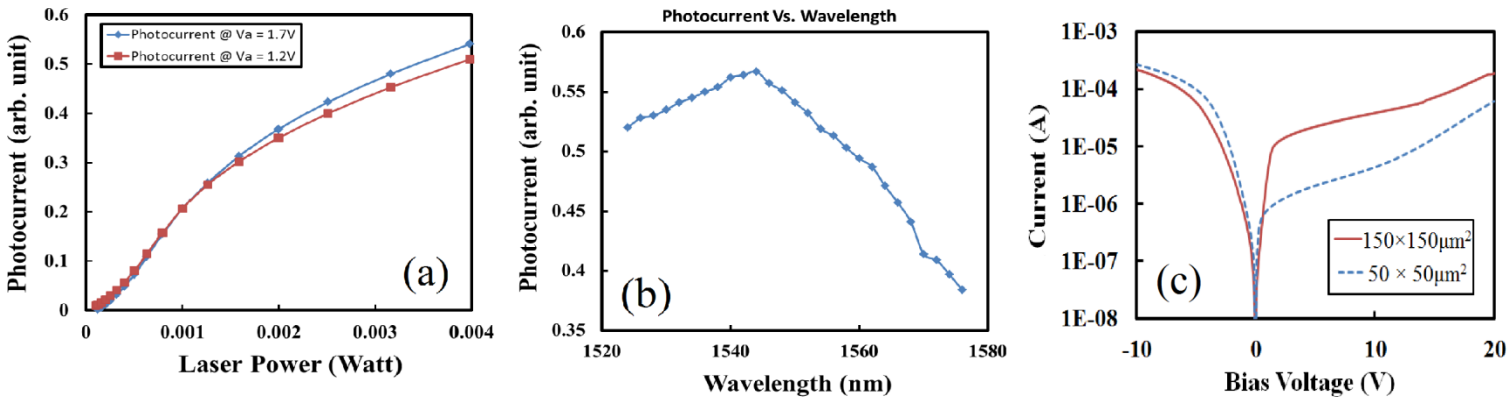

Fig.4. Shows the photocurrent measurements versus (a) laser power at 1.2V and 1.7V bias, and (b) laser wavelength at 1.2V bias. (c) Shows the current measurements in darkness.