Student Paper

Mobility Determination through a Two Mask 'Gridded' Capacitor Structure

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We present a method to extract the inversion mobility from a capacitor structure. The method employs a 'gridded' capacitor to supply minority carriers, thereby, alleviating the need to fabricate a transistor with source/drain contacts. This structure requires only two masks. Although we use silicon as a starting material, this method is versatile and can be employed for other substrate materials.

Our gridded capacitors use a silicon oxide (SiO_2) tunnel oxide, a silicon nitride (Si_3N_4) charge trapping region, and an aluminum oxide (Al_2O_3), shown in Figure 1. First a p-type substrate undergoes a photolithography step to define the grid. The grid is doped with the opposite carrier type from the substrate. A typical grid structure consists of line widths of 5um and line spacing's, L, ranging from 30µm to 300µm. Next the gate stack is grown/deposited. Our gate stack consisted of three dielectrics for non-volatile memory studies; however, any gate stack can be used. Metal contracts of aluminum are made to the back of the substrate as well as the gate stack. The capacitors, which range from radiui of 40µm to 250µm, are defined with a final photolithography step and metal etch.

A transistor can be analyzed with transmission line theory applied to Fig. 2 [1]. The analysis shows the inversion carrier mobility extracted from a conductance measurement can be defined as:

$$\mu_{inv} = \frac{\omega_p L^2}{4(2.54)(V_{GS}-V_{TH})} \quad (1)$$

where ω_p is the peak radian frequency in the conductance measurement. Previously, we have applied this method to a SONOS transistor device and have obtained agreement between the inversion mobility defined in Eqn. 1 and the transistor mobility measured at low drain voltages [2]. The 'gridded' capacitor technique varies the L dimension, where the grid acts as a source and drain for minority carriers to provide an equivalent resistance and length as shown in Fig. 3. The inversion carrier mobility becomes

$$\mu_{eff} \approx \left(\frac{1+\sqrt{2}}{2}\right)^3 \frac{\omega_p L^2}{4(2.54)(V_{GS}-V_{TH})} \quad (2)$$

A conductance vs. frequency at $V_{GS} - V_{TH} = 2V$ on a 100µm radius capacitor on a 50µm grid spacing is shown in Fig. 4. The 'gridded' capacitor exhibits a peak at f_p=9.6MHz which corresponds to an inversion mobility of 369 cm^2/V-s. In summary, we have shown a 'gridded' capacitor may be used to determine the inversion carrier mobility. This structure requires only two masks and alleviates the need for source and drain contacts. Although, we have demonstrated its usefulness on silicon devices; the method is well-suited to other material systems, such as high mobility III-V devices, graphene [3], or carbon nanotubes.

References

[1] P. D. Chow and K. L. Wang, "A new AC technique for accurate determination of channel charge and mobility in very thin gate MOSFETs," *IEEE Trans. on Elect, Dev.*, **33**, 1299 (1986)

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[3] B. C. Huang, M. Zhang, Y. Wang, and J. Woo, "Contact resistance in top gated graphene field-effect transistors," *Applied Physics Letters* **99**, 032107, (2011)

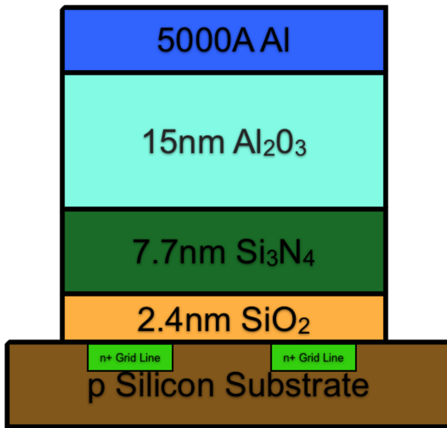

Fig. 1 Cross-section of the gate stack with a 2.4nm SiO2 tunnel oxide, 7.7nm charge trap Si3N4 layer, and a 15nm Al2O3 blocking oxide layer.

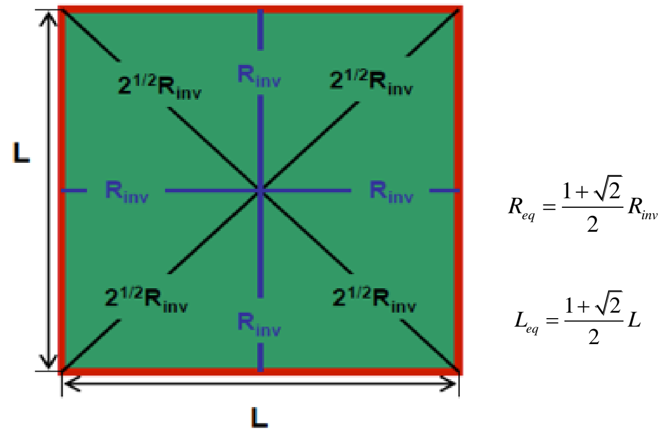

Fig. 2 Equivalent resistance and length of a gridded capacitor square for mobility determination

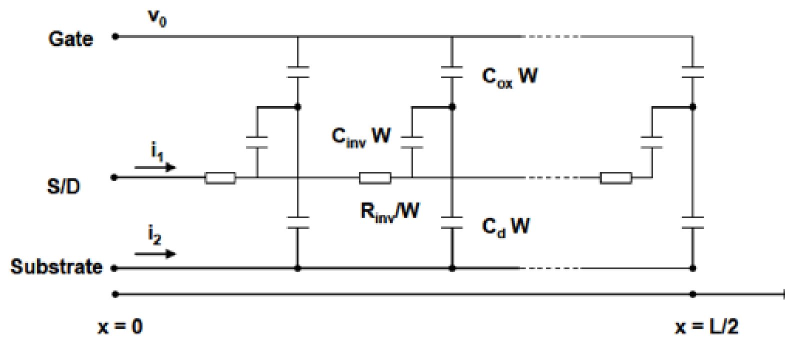

Fig. 3 Transmission line equivalent circuit for a transistor device. The two currents i_1 and i_2 can be used to find the inversion layer mobility from a two terminal setup [1]

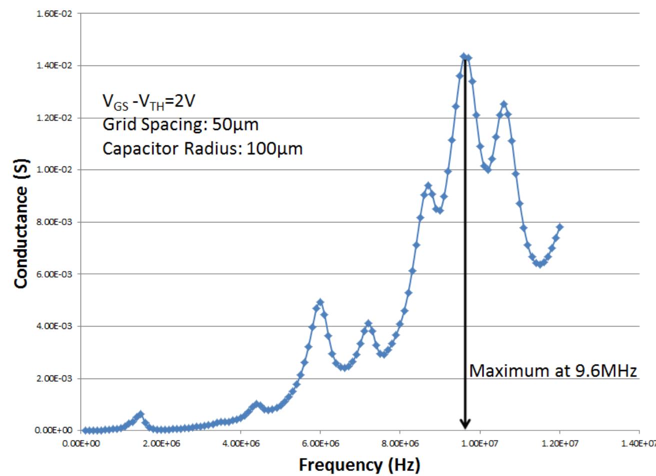

Fig. 4 Conductance vs Frequency of the gridded capacitor completed on a 100µm capacitor radius, 50µm grid spacing at a bias of 2V. The maximum occurs at 9.6MHz which corresponds to an inversion layer mobility of 369 cm^2/V-s