Back-End-of-Line Test Structure Design and Simulation for Subsurface Metrology with Scanning Probe Microscopy*

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As demands in the semiconductor industry call for further miniaturization and performance enhancement of electronic systems, the traditional planar (2D) electronic interconnection and packaging technologies show their difficulties in meeting the ever-advancing standards of the industry. To overcome such limitations, 3D stacked integrated circuits (3D-SICs) draw tremendous research interest and have been widely studied.[1] In the end, the billions of transistors are interconnected with tens of kilometers of wires that packed into an area of square centimeters, making a giant "metallic forest".[2-4] The complexity of the multi metallization levels of back-end of line (BEOL) brings challenges such as resistive-capacitive (RC) delay and reliability issues.

From the metrology point of view, traditional scanning probe microscopy (SPM) technologies show mature capabilities of acquiring the surface metrology. However, additional capabilities such as subsurface imaging and electromagnetic property extraction in nano-scale are required to solve BEOL problems. Recently, several techniques, such as scanning microwave microscopy (SMM), electrostatic force microscopy (EFM) and Kelvin probe force microscopy (KFM) have shown their promising capability of subsurface characterization on different semiconductor devices. [5, 6]

To enhance our SPM subsurface metrology capabilities and determine more accurately the limitations of the technique, we will compare experimental and simulation results. A multi-level test chip with several well-known buried structures has been designed and will be integrated on a thumb-nail size chip. Pads will be bonded on a printed circuit board (PCB), allowing external bias accesses. Different feature components can be biased separately to simulate a device under test (DUT).

In this work, the surface potential distributions of opposite biased parallel buried metal lines are simulated to estimate the KFM subsurface resolution under different line depth and separation. COMSOL Multiphysics** has been used to create the basic three-wire system (Fig. 1(b)), which presents the basic parallel finger structure in Fig.1(a) The three wires are aluminum which are submerged in a glass substrate. The two outer wires are biased with 1V while the middle wire is biased with -1 V. 20 nm above the substrate, a real-size conical conductive platinum tip with a 10 nm terminal radius is constructed to simulate the apex of the KFM probe. The floating potential variation of the tip has been observed as tip moves through a perpendicular line across the wires. Two main extreme parameters in our chip design process have been compared:

1) Fig. 2(a) simulates the deepest buried line position. It shows the tip potential has only little fluctuation within the depth of 4.8 um. This limits the KFM resolution, which used to sense the surface potential.

2) Fig. 2(b) simulates the closest line position. It shows a decent KFM resolution can be expected with the depth up to 1.6 um while no potential resolution can be detected in the depth of 4.8 um.

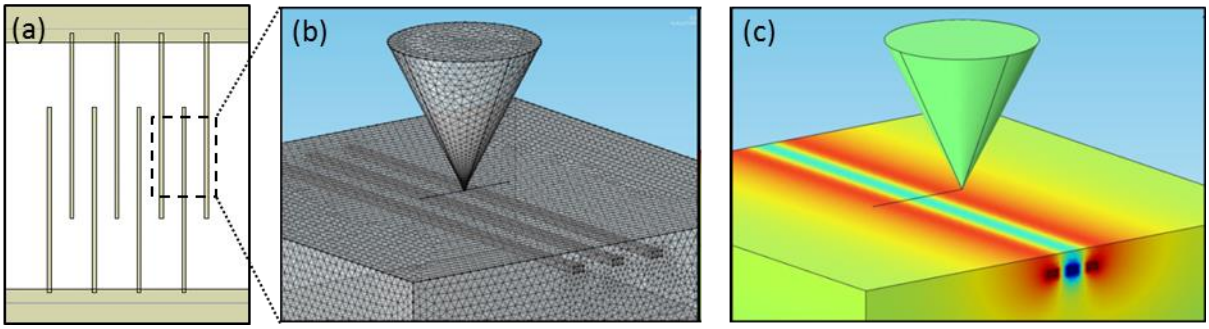

Fig.1 (a) Test structure layout (Part), (b) Meshing of Simulation Geometry, (c) Visualization of the Electric Potential.

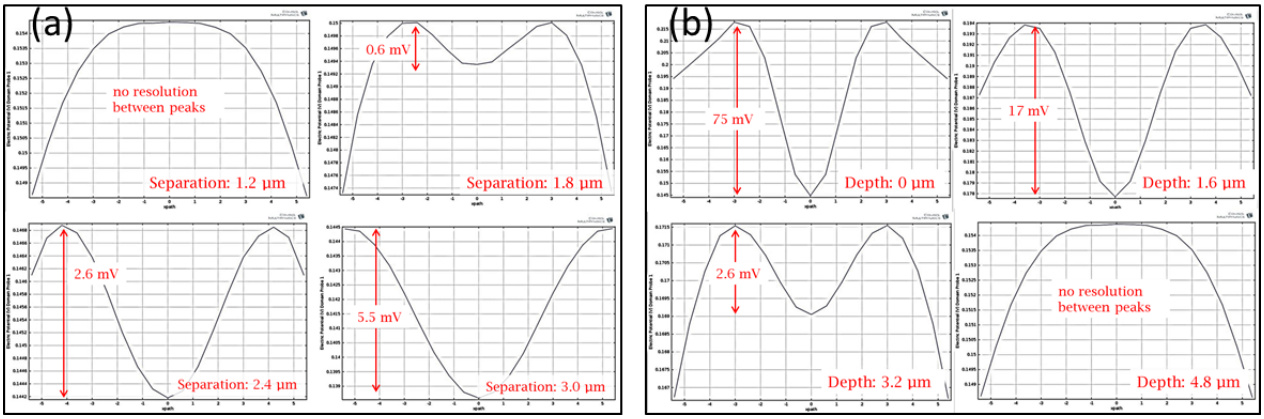

Fig.2 (a) Surface Potential Distribution at Various Wire Separations, Wires at 4.8 µm Depth,
(b) Surface Potential Distribution at Various Wire Depths, Wires at 1.2 µm Separation.

References

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NOTE

** Certain commercial equipment, instruments, or materials are identified in this paper in order to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by NIST, nor does it imply that the materials or equipment used are necessarily the best available for the purpose.