Student Paper

Comprehensive Analysis of Ultra-Thin-Body MOSFETs for Monolithic 3D Logic Circuits With Interlayer Coupling

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Introduction: Monolithic 3D integration, which sequentially stacks multiple active layers with dense inter-tier vias, enables the full use of the third dimension to enhance performance and packing density [1-4]. Currently, the performance benefits of monolithic 3D technology have been shown to mainly come from its shorter interconnection which contributes to smaller RC delay [3]. However, the electrical coupling through the thin interlayer dielectric (Fig. 1(a)) may alter the characteristics of upper transistors [1] and the resulting impacts on various monolithic 3D logic circuits merit detailed examination. Considering interlayer coupling and real layouts, this work indicates that substantial performance improvements are achievable in monolithic 3D inverter, 2-Way NAND and 2-To-1 MUX, particularly for operations at lower V_{DD}.

Evaluation Framework: Double-tier 3D circuit design, one for NFET and the other for PFET, is adopted with nano-scale inter-tier vias locally connecting internal nodes and metal lines at distinct layers (Fig. 1(b)). For comparison, we utilize dual reverse body biases (V_{BG} = 0V and V_{DD} for NFET/PFET, respectively) for planar 2D circuits to minimize the overall leakage. For 3D circuits, the V_{BG} of bottom layer is reversely biased if not otherwise mentioned. In Fig. 2, the impact of V_{BG} on I_D modulation is evaluated for SOI Ultra-Thin-Body (UTB) devices with various buried oxide thickness (T_{BOX}). Due to its enhanced electrical coupling, modulation efficiency increases with thinner T_{BOX}, especially for the cases at lower V_{GS} where I_D is exponentially dependent on the change in V_T.

Leakage/Delay of 2D/3D Logic Circuits: Fig. 3 compares the leakages between 2D/3D inverter at various V_{DD}. The monolithic 3D inverters, with identical reverse V_{BG} configurations of the device in dominant leakage path (Fig. 3(b)), offer minimum leakage for each layer combination without extra area overhead as in the planar 2D design of using dual V_{BG}. In Fig. 4(a), because of the enhanced strength of upper-tier transistors, 3D stacked inverters exhibit better output falling and rising performance for (Top/Bottom) tier = (N/P) and (P/N), respectively. With rising and falling transitions occurring simultaneously, Fig. 4(b) shows that monolithic 3D 5-stage inverter chain exhibits performance improvements for each tier design.

For monolithic 3D 2-Way NAND, direct (case (I)) and switch (case (II)) gate alignments between the tiers are assessed (Fig. 5). At V_{DD} = 1.0V, significantly larger leakages are observed for the case (II) design with input pattern (A,B) = (0,1) and (1,0). The aggravated leakage results from the OFF transistors (NFET with input A or B) with forward V_{BG} coupling from the bottom transistors. For delay analysis (Fig. 6), 3D 2-Way NAND stacked with (N/P)-tier design increases the strength of NFETs, thus allowing faster bottom switching and better performance. In Fig. 7, the case (I) and (II) layout designs of 3D 2-To-1 MUX stand for the gate alignment of upper and bottom transistors with identical and complementary signal, respectively. For 2-To-1 MUX leakage analysis, the OFF transmission gate dominates the overall leakage. As such, the case (II) layout that designs with complementary front-gate voltage (V_{FG}) and V_{BG} for upper devices suffers higher leakage while the case (I) design, with modifications in 3D layout, appears to be a better choice to minimize leakage. In Fig. 8, the (N/P) and (P/N) tier configurations of 2-To-1 MUX exhibit delay improvement in passing "0" and "1" which is related to the strength of NFET and PFET, respectively. Fig. 9 shows the layout of a two-tier 3D 2-To-1 MUX with case (I) design. For the case (I) design that possesses superior performance and leakage, extra metal routing to connect the input signals (D0 or D1) of top and bottom transistors in each transmission gate occupies larger area (20% overhead compared with the case (II) design).

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Reference: [1] P. Batude et al., *IEDM*, p. 345, 2009. [2] T. Irisawa et al., *VLSI Tech.*, p. 56, 2011. [3] Y.-J. Lee et al., *ICCAD*, p. 539, 2012. [4] S.-M. Jung et al., *VLSI Tech.*, p. 220, 2005.

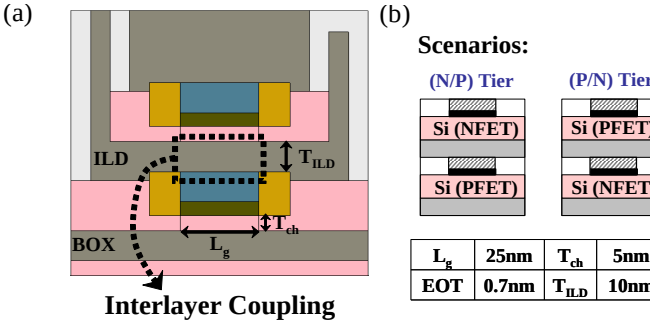

Fig. 1. (a) Two-tier monolithic 3D stacking showing the electrical coupling between tiers and (b) the scenarios with various tier combinations and device geometries.

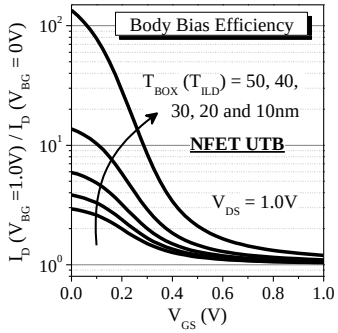

Fig. 2. Comparison of body bias (V_{BG}) efficiency for NFET UTB devices with various buried oxide thickness (T_{BOX}).

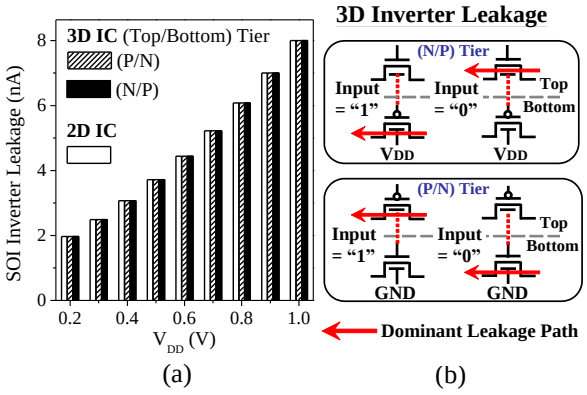

Fig. 3. (a) Leakage comparison of 2D/3D SOI inverter at various V_{DD}, and (b) the schematic showing the dominant leakage path of 3D inverter with reverse V_{BG} as in the optimized 2D design.

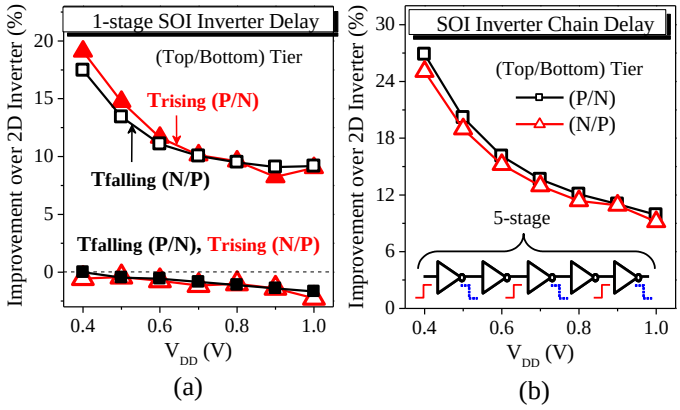

Fig. 4. (a) Delay comparison of 2D/3D 1-stage inverter. (b) The monolithic 3D 5-stage inverter chain offers better performance for each tier combination.

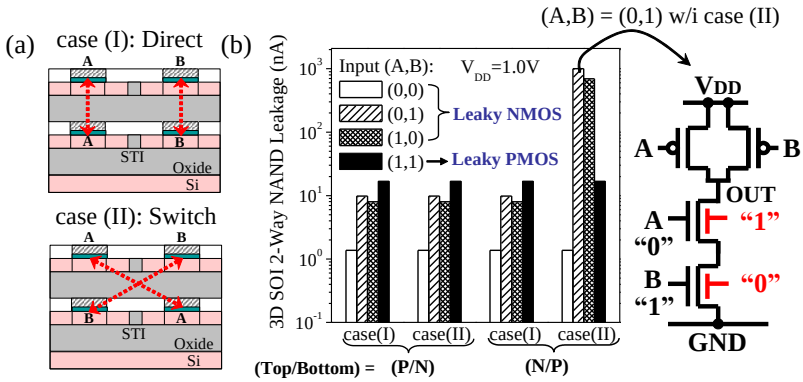

Fig. 5. (a) Definition of 3D layouts with distinct V_{BG} connection among the tiers for monolithic 3D 2-Way NAND, and (b) the leakage comparison between different tier combinations and input patterns.

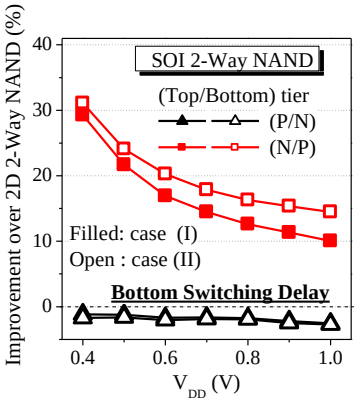

Fig. 6. Delay comparison of 2-Way NAND integrating with planar 2D and monolithic 3D designs.

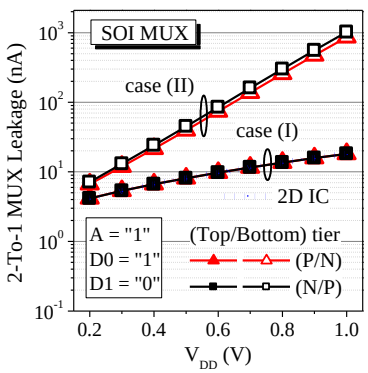

Fig. 7. Leakage comparison of planar 2D and 3D 2-To-1 MUX with case (I) and (II) layout designs.

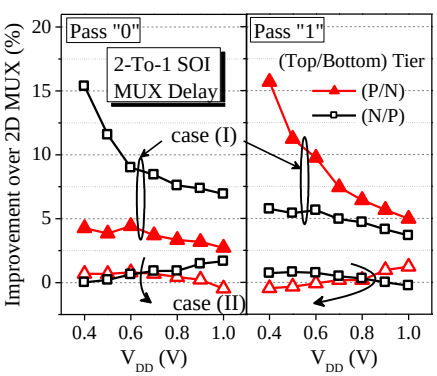

Fig. 8. Delay comparison of 2-To-1 MUX with 2D/3D designs.

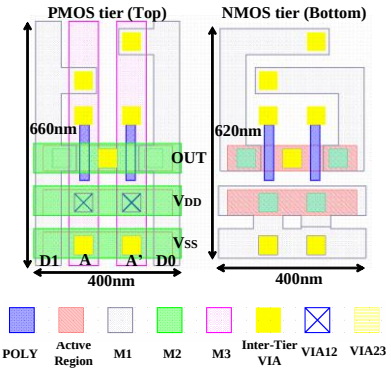

Fig. 9. Layout of two-tier 3D 2-To-1 MUX with case (I) design in (P/N) tier scheme.