Student Paper

Design of Complementary Field-Effect-Diode Transistors with Buried Back-Gates

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With the development of Silicon-on-insulator (SOI) technology, ultra-thin-body transistors and gate-all-around transistors have been proposed to suppress the short channel effects. In order to further improve the operation frequency, Field-Effect-Diode (FED) transistor has been proposed. The FED transistor works as a forward-biased diode when it is switched on, as results in an exponential increase of drain current in its output characteristics. High frequency operation [1, 2] and memory application [3] of FED transistors have been explored. However, the FED transistor requires two gates above the channel region, as increases the device dimension and the fabrication complexity. In this paper, we investigated an FED transistor with a buried back-gate and a front-gate by simulation. Merits of high on/off ratio, complementary behavior, and high process compatibility are demonstrated.

The proposed n-type FED transistor with a buried back-gate in this paper is shown in Fig. 1a. It has two gates, one on the front side and controls the switching of the device. The back-gate is buried in the substrate as heavily doped region, which can form a reverse-biased pn junction in the substrate of SOI wafer. The voltage-drop across the junction will influence the potential of the thin device body. L_{FG} and L_{BG} represent the lengths of these front-gate and back-gate, respectively. The back-gate voltage V_{BG} is fixed during operation. This device can operate as a switch with the changing of the front-gate voltage V_{FG}, which results in on-state and off-state of the device. At the on-state, the device behaves as a forward-biased pn junction diode. At the off-state, it behaves as a turned-off p-n-p-n thyristor. Fig. 2 shows the band diagram of n-type FED transistor with a positive V_{BG}, zero-biased V_{FG} and positive drain voltage V_D. Energy bands are pulled down by a positive V_{BG} and a higher barrier in the reverse-biased pn junction of the thyristor structure is formed. The drain current is dramatically reduced and the device is turned off with V_{FG} of zero volt. With an increased V_{FG}, an n-type channel is formed and device will be switched on. The output characteristics of n-type FED are shown in Fig. 3, where a diode-like behavior can be seen with the increased drain voltage V_D.

The impacts of drain voltage, back-gate voltage, length of the back-gate and thickness of the device silicon layer on device performance are investigated by Sentaurus TCAD simulation. As shown in Fig. 4a, the device drive current increases with the increasing L_{BG}. In Fig. 4b, a thinner device layer leads to a lower leakage. In Fig.5, the leakage current can be reduced by increasing V_{BG} by forming a reverse-biased pn junction of the pnpn structure. Meanwhile, drive current will be almost the same when a sufficient V_{BG} value is provided. We also investigated the complementary FED transistors. As shown in Fig. 1b, the p-type FED transistor is realized by changing the doping polarity. Complementary electrical properties can be achieved in Fig. 6. The process flow for fabricating the complementary FED transistors is summarized in Fig. 7. The buried back-gate region can be realized by ion implantation and the process flow is compatible with the conventional CMOS process,

In conclusion, complementary FED transistors with buried back-gates are proposed. The merits of high on/off ratio, large drive current, low leakage current, and complementary structure make it possible for high speed and low power logic applications.

References

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[3] I.Sheikhian and F. Raissii,"High-speed digital family using field effect diode," *Electron. Lett.*, vol. 39, no. 4, pp. 345-347, Feb 2003.

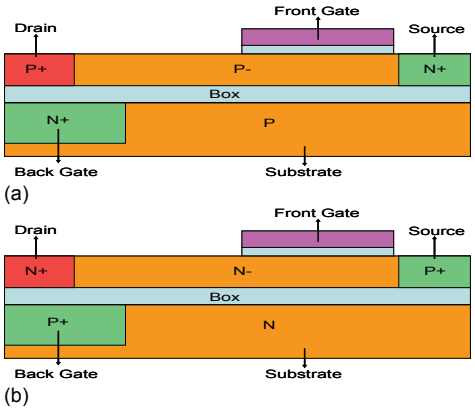

Fig. 1: Schematic of the complementary FED with a doped back substrate: (a) n-type FED transistor.(W_{poly}=5.07eV) (b) p-type FED transistor. (W_{poly}=4.13eV)

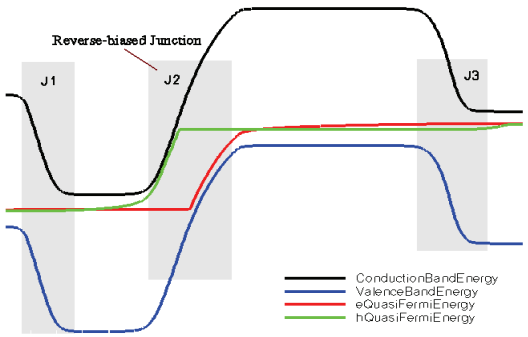

Fig. 2: Band diagram of the FED at positive V_{BG}, zero-biased V_{FG}, positive V_D. It shows an off-state FED which is a thyristor structure with a reverse-biased pn junction in the middle.

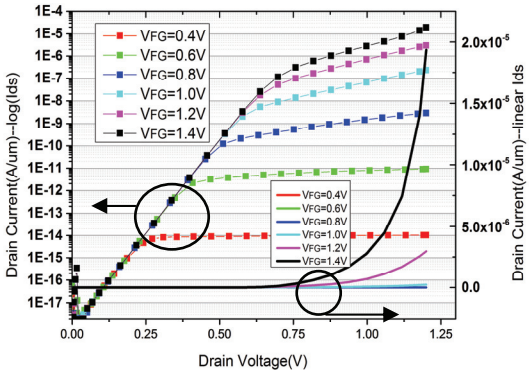

Fig. 3: Output characteristics (I_D-V_D curve) of the n-type FED transistor. With the increasing front-gate voltage, the FED is turned from off-state to on-state. (V_{BG}=2V)

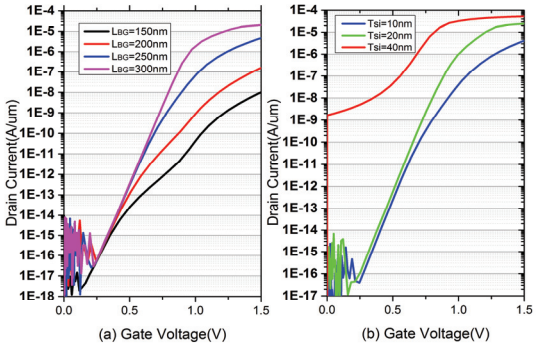

Fig. 4: (a) I_D-V_{FG} curve with different lengths of back gate. A longer lateral length of back gate leads to a larger drive current. (b) I_D-V_{FG} curve with different thickness of device silicon on insulator. A thinner silicon layer leads to a lower leakage. (V_{BG}=2V, V_D=1V)

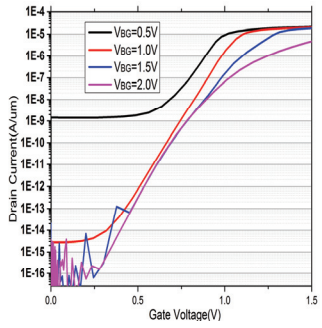

Fig. 5: I_D-V_{FG} curve with different back-gate voltages. It shows that an increased back-gate voltage can reduce off-state leakage current and a weak influence of drive current in on-state can be seen. (V_D=1V)

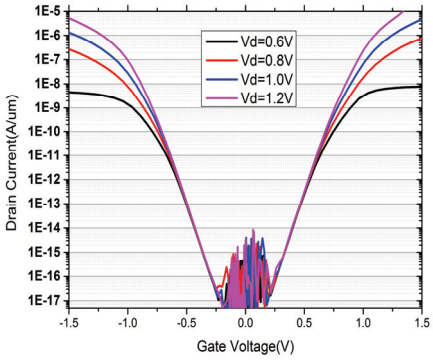

Fig. 6: I_D-V_{FG} curve (transfer I-V curve) of complementary FED transistors. It shows that complementary FED transistors can obtain complementary electrical behavior.

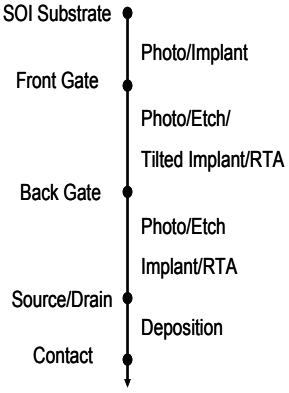

Fig. 7: A brief summary of the fabrication process flow of FED transistor with a doped back-gate. Back-gate of the device can be achieved by tilted ion implantation.