Student Paper

Single Event Upset Mapping of DICE SRAM Cells

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***Abstract*—In this paper the single-event-upset sensitive information of DICE SRAM is analyzed. This experiment is based on backside laser test and heavy ions experiment. The SRAM device is directly bonded to PCB prepared for the laser testing without package. The laser energy thresholds for SEU for 4-Mbit SRAMs fabricated in 0.18-um technology are measured using 1064nm pulsed laser. Laser SEU sensitivity mapping at the cell level is also under investigation in consideration with depth factor, finally three-dimensional SEU sensitive volume is obtained. The laser measurements are modified by heavy-ion threshold LET measurements to determine an empirical relationship between laser energy and heavy-ion LET. This empirical relationship is used as the scale of the SEU sensitivity mapping of SRAMS. The laser sensitive information can help designer modify the hardened structure.**

Index Terms—**Chip on board (COB), Laser, single event effects (SEE), single event upset (SEU), SRAM.**

I. Introduction

THe storage device applied in the spacecraft would be upset when it is hit by heavy ion. The pulsed laser method usually develop focusing a laser beam with a spot size less than 1 um on to the surface of the device under test allowing investigation with a three-dimensional resolution. However for the large scale integrated (LSI) circuits, opposite to a heavy ion, the laser beam is difficult or even impossible to penetrate through metal layer focusing on the active area of the device. Backside laser experiment is developed to eliminate the effect of metallization lays, which laser beam strikes the backside of device. [1].

In present work, we use pulse laser facility and heavy-ions accelerator testing to analyze the SEU sensitivity of DICE SRAM chips. First the laser energy thresholds for SEU are obtained. Secondly, we develop the heavy-ion experiments to get heavy-ion threshold LETs and the cross section of the chip. Finally, we scan some cells formed in DICE structure of SRAM in detail to obtain the laser SEU sensitivity mapping of chips at the cell level. We also analyze the depth of the sensitive volume; therefore three-dimension SEU sensitive map finally can be obtained.

II. Device Under Test and Test Procedure

The SRAM device under test (4M×8) is fabricated in standard 180nm CMOS technology and is consisted of 12T DICE cell. The DICE memory cell is shown in Fig 2. The architecture contains four memory nodes Q1, Q2, Q3 and Q4 to storage data, by connecting the output and the input of four inverters in an interleaved feedback configuration. The data of the node will revert by the feedback of other three nodes, when only one node is striking and storage

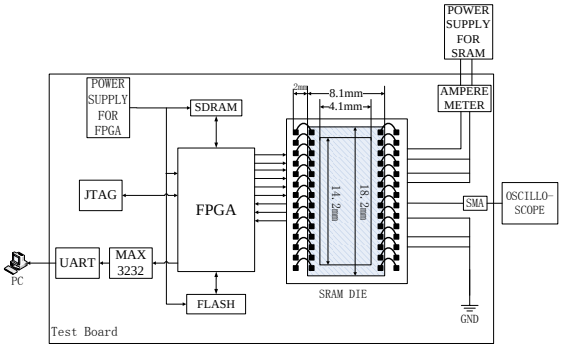

Fig 1 Laser test Print Circuit Board (PCB)

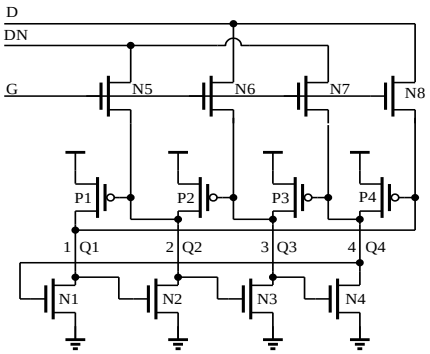

Fig 2 Schematic of the DICE cell

voltage is changed. Therefore DICE design is considered immune to only one storage node upset. However, multiple storage nodes in the DICE architecture can collect charge during one single ion striking due to the charge sharing, as a result, the data of the storage cell would upset. In this paper, we will analyze the SEU sensitivity of the memory cell using 1064 pulsed laser [10, 11]. The SRAM is tested as shown in Fig 1.

III. EXPERIMENT RESULT

The sensitivity map for the SRAM memory cell is shown in Fig. 3. The regions with blue color have lower SEU threshold which less pulsed laser energy is required to prevail upsets; the regions with gray color have higher threshold which more pulsed laser energy is required to prevail upsets. The colors between them signify the different SEU threshold energy. The total area under scanning of the sensitivity map is a rectangle with the size 20um×20um, which contains two memory cells (size of the basic cell is about $\sim 6um \times \sim 12u$).

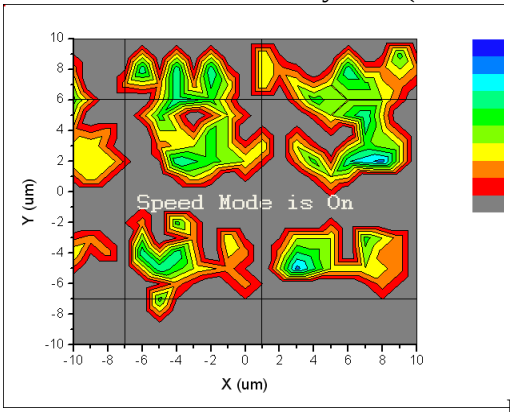

Fig 3 SEU Mapping of the DICE SRAM

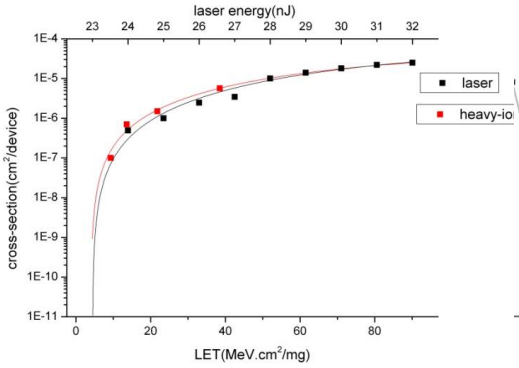

Fig 4 The Cross Section of Heavy ion (the curve with red color) and pulsed laser (the curve with black color)

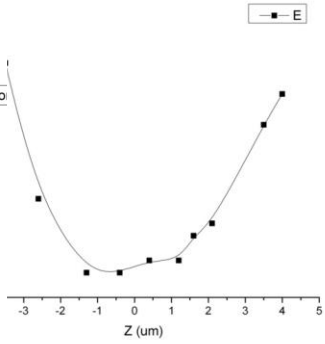

Fig 5 The Depth profile of the sensitive volume

The pulsed laser SEU cross section is obtained experimentally using the method detail in [2] and [3]. The cross section is computed through the total area of scanning laser spots that induce upsets. The ' in this case is defined as:

$$\sigma_L(E_L) = N_E(E_L)\frac{S}{M \times N}$$

Where $N_E(E$ is the number of the upsets observed for a given pulsed laser energy in scanning area, S is the size of laser scanning area, $M \times$ is the number of laser spot in scanning area. To correlate the laser work with the heavy ion experiment, the SEU cross section of pulsed laser is produced and compare with that of heavy ion. As shown in Fig. 4. There are two curves, one is the cross section of pulsed laser, and the other is that of heavy ion. We choose a single point near the center of SEU sensitivity maximum to analyze the SEU sensitivity with the dimension of depth and the depth of laser focus is varied. The width of the SEU sensitivity in Z direction is derived in Fig. 5 with a sensitive layer that is approximately a few micrometers. In the thickness between them about 3 micrometers, the threshold energy is almost constant.

IV. Conclusion

These experiments show the SEU sensitive information of the DICE SRAM circuit in cell level and the SEU threshold energy map is also obtained which can help analyze SEU capability of DICE structure fabricated in standard 180nm CMOS technology. There are some areas without sensitive pairs are invulnerable of pulse laser. We will analyze the critical distance of sensitive nodes that cannot collect charge together in the future, which has meaning on the composition of layout.

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