Synthetic Electric Field Tunnel FinFET Achieving both High ON Current and Low Sub-Threshold Swing at Low Drain Voltage

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The tunnel FET (TFET) is one of the most promising low-power-consumption devices. To realize low voltage operation with sufficient on/off performance, enhancement of the electrostatic controllability is one of the most significant factors. In the case of a conventional metal-oxide-semiconductor FET (MOSFET), 3D transistor architectures such as a "FinFET" are regarded as excellent solutions. As for the "tunnel FinFET" approach, fin-width scaling [1], or tuning the threshold voltage using dual gates [2] has been demonstrated.

In the present study, to obtain further improved electrostatic controllability, we propose a novel double-layer tunnel FinFET architecture, which initiates synthetic electric field effects to improve TFET performance. The effectiveness of the architecture and the resulting performance are investigated.

The synthetic electric field (SE) effect, which enhances TFET performance, is realized by an ultrathin undoped channel deposited on the heavily-doped source well and a wrap-around gate electrode [3]. (Fig. 1) The gate electrode induces both orthogonal and parallel electric fields at the vertical tunnel junction. The electric field is intensified by the multiplication effect of both top and side gate electric fields and initiates enhanced potential modulation at the tunnel junction. The SE effect is further enhanced by scaling the device dimensions [4]. (Fig. 2) When the channel dimensions D_{EPI} and W_{CH} are 50-nm-thick and 50-nm-wide, respectively, the maximum electric field is small and is only caused by the orthogonal electric field. Thinning the channel thickness to 10 nm increases the parallel electric field, and the maximum electric field is increased. This effect is also enhanced when the channel width is scaled from 50 nm to 20 nm (top curve). This suggests that slim and scaled devices like a tunnel FinFET are advantageous for obtaining the SE effect. In Fig. 1, a double-layer tunnel FinFET is characterized by the fin-width (W_{FIN}), channel-thickness (D_{EPI}), and source overlap length (L_{OV}). Fig. 3 shows a device fabrication flow. Source and drain regions were initially formed in the silicon-on-insulator (SOI) wafers by the ion implantation (I/I) technique. Next, an ultra-thin epitaxial Si channel was deposited using vapor phase epitaxy. After the preferential fabrication of the epitaxial channel/source tunnel junction, fin-patterning was carried out. A HfO_2 gate insulator and a TiN gate electrode were deposited. Cross sectional transmission electron microscopy (X-TEM) images reveal that a thin epitaxial channel is directly grown on a highly-doped source surface with negligible defects, and the gate electrode is surrounding the double-layer fin channel (Fig. 4). The epitaxial channel contributes to the excellent abruptness of the dopant profile that is as small as 1 nm/decade. [3,5,6]

The trend of performance improvement shown in the experimental results is confirmed in the I_D–V_G characteristics with fin-width scaling (Fig. 5). The increase of I_D and the improvement of sub-threshold swing are remarkable for narrow fin channels. In the I_D–W_{FIN} relationship, the current portion at the fin-sidewall, which is indicated by I_D at $W_{FIN} = 0$, is remarkably large. (Fig. 6) By reducing W_{FIN}, performance of the TFET is enhanced. Fig. 7 shows I_D–V_G and I_D–V_D characteristics of the SE tunnel FinFET with a 12-nm-W_{FIN}, a 7-nm-D_{EPI}, and a 25-nm-D_{SOI}. Here we need to mention that, even at very low V_D (−0.2 V), excellent on/off performance can be realized. Significant I_D values of 4 uA/um (V_G = −0.5 V) or 40 uA/um (V_G = −1 V) are also obtained with a sub-threshold swing of 58 mV/dec at a V_D of −0.2 V. These features are a great advantage of the SE-TFETs for potential low voltage operation. Strong gate controllability initiated by the SE-effect around the tunnel junction could be the origin of the significant performance observed. Future step-by-step performance boosts could be expected by adopting booster technologies or by replacing the channel material to Ge or III-V semiconductors.

Acknowledgements
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References

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[4] HyENEXSS ver. 5.5

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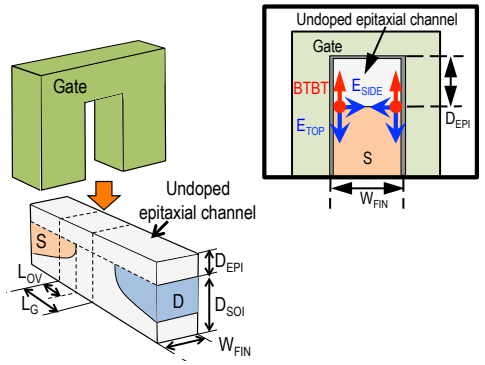
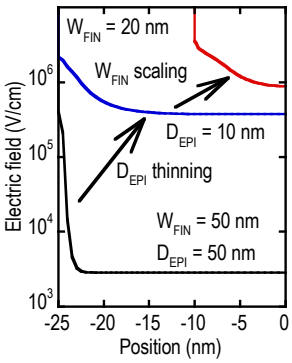
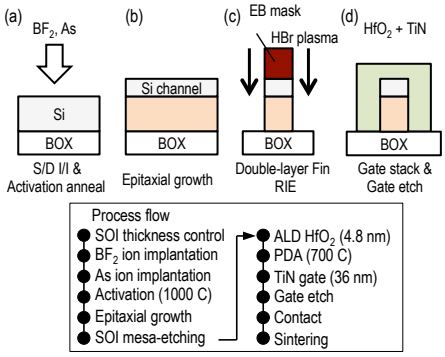


Fig. 1 Device structure of SE-tunnel FinFET. Based on the FinFET-like structure, the ultrathin undoped channel is stacked on a heavily-doped source well, which is wrapped around by the gate electrode. The cross-section of the double-layer Fin channel is shown inset.



Φγ. 2 Ιμ παχτσοφχηαννελδιμ ενσιονσ on the electric fields at the tunnel junction in SE-tunnel FinFET (simulation). Position represents the thickness from Fin-sidewall surface at the vertical source/channel interface.



Φγ. 3 Σχηεμ αχ προχεσσφοω οφ τηε SE-tunnel FinFET with the S/D-first and tunnel-junction-last processes.

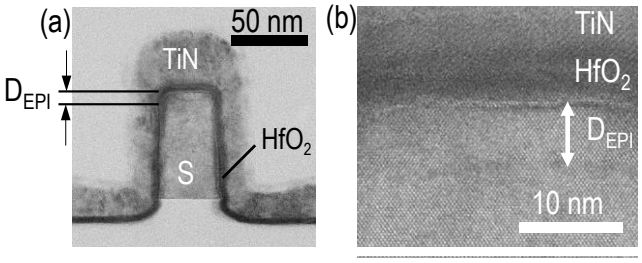


Fig. 4 Typical X-TEM images of the SE-tunnel FinFET. (a) Channel cross-section, and (b) Magnified epitaxial channel interface.

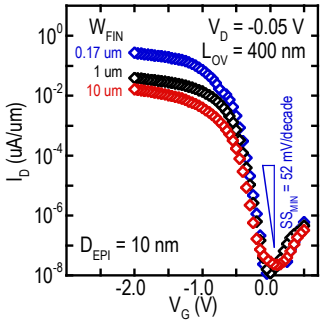


Fig.5 Comparison of I_D–V_G characteristics (V_D= □0.05 ς) ωιτη Φν ωιδτησ 170, 1000, ανδ 10000νμ .

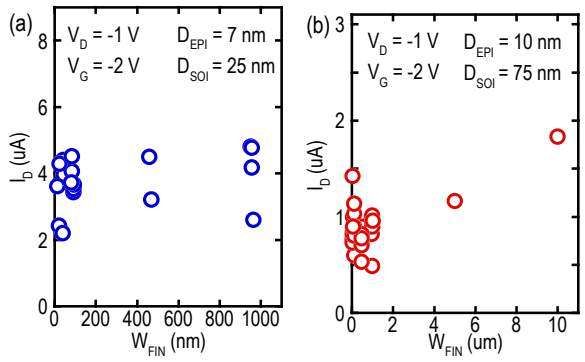


Fig. 6 Measured I_D–W_{FIN} relationships of the p-type SE-tunnel FinFETs. V_G and V_D οφε □2 ανδ □1ς , ρεσπεχτιελψ

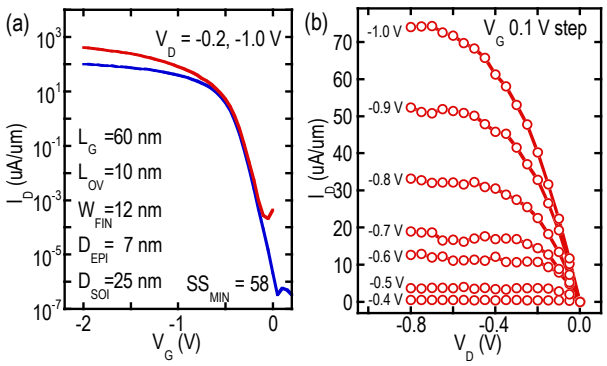


Fig. 7 Normalized (a) I_D–V_G and (b) I_D–V_D characteristics of SE-tunnel FinFET with scaled W_{FIN}, D_{EPI} and D_{SOI}.