Invited Paper

III-V Nanowire Transistors for Low Power Electronics

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III-V channel materials are currently being considered as enablers for further CMOS improvement in the near future, with the ITRS roadmap indicating an introduction around 2019. The high electron mobility allows for close to ballistic transport even at fairly long gate lengths L_g ~30 nm, as demonstrated in InP-based HEMTs. Current improvements in high-k III-V interfaces have substantially improved D_{it} levels during the last few years, which has yielded impressive III-V MOS performance. Transistors with very high g_m=2.45 mS/µm [1], low R_{on}=199 Ωµm [2] and high f_T/f_{max} (255/355 GHz) and subthreshold slopes below 80mV/decade [3].

Further, multi-gate or gate-all-around gate geometries gives better electrostatic control as compared with planar transistors. The better gate coupling suppresses short channel effects, and thus improves the sub threshold slope and the output conductance. For example, for Si-CMOS the self gain ($g_m r_0$) improved from 6 to 14 when going from a planar to a tri-gate geometry. Etched InGaAs gate all around wires have shown excellent performance, with g_m= 1.74mS/µm and SS=63mV/decade [4] .

We have developed methods of fabricating $In_xGa_{1-x}As$ nanowires using selective MOCVD growth, both in vertical and lateral geometries, both showing very promising device performance. These approaches avoids any dry etch schemes, and can thus avoid any etch related damage.

The vertical device geometry is based on a vapor-liquid-solid growth method [5]. Starting on a 300 nm thick InAs n^+ buffer on highly resistive Si, InAs nanowires are grown vertical from the surface through the use of Au gold discs. In this way, wires with diameters 20-50 nm with lengths 300nm-800nm are grown. The wires are further doped during the growth using Sn. After the growth, the wires are coated with an Al_2O_3/HfO_2 high-k oxide using ALD. Spacer layers, tungsten gates and source/drain ohmics are further fabricated using CVD/sputtering and etch back techniques. Figure 1a shows a cross section image of a vertical nanowire FET.

Our lateral nanowire process uses a dual step HSQ hard masks formed on a S.I. InP substrate [6], based on planar InGaAs MOSFET process [2]. First, HSQ lines (widths 30nm, spacing 30 nm) are exposed using EBL. InGaAs fins are then selectively grown using MOCVD. A second HSQ step is then used for protecting the gate part of the wires, after which a second growth step is used for growth of n^+ InGaAs contacts. Figure 1b shows a top view of InGaAs wires between the two n^+ contacts. After high-k deposition, a self aligned T-gate is subsequently formed to the nanowires, forming tri-gate transistors. Self aligned source/drain ohmic contacts are subsequently deposited.

The vertical nanowire transistors have displayed a maximum g_m=1.34 mS/µm at V_{ds}=0.5 V and g_m=1.8 mS/µm at V_{ds}=1.0 V, for transistors consisting of a single nanowire with L_g=200 nm. The minimum on resistance is R_{on}=280 Ωµm. These are excellent values considering the fairly long gate length, indicating good transport properties of the InAs wires. For array FETs consisting of several wires

in parallel (192), transconductance drops to around g_m=0.4 mS/µm, partly due to extrinsic source resistance.

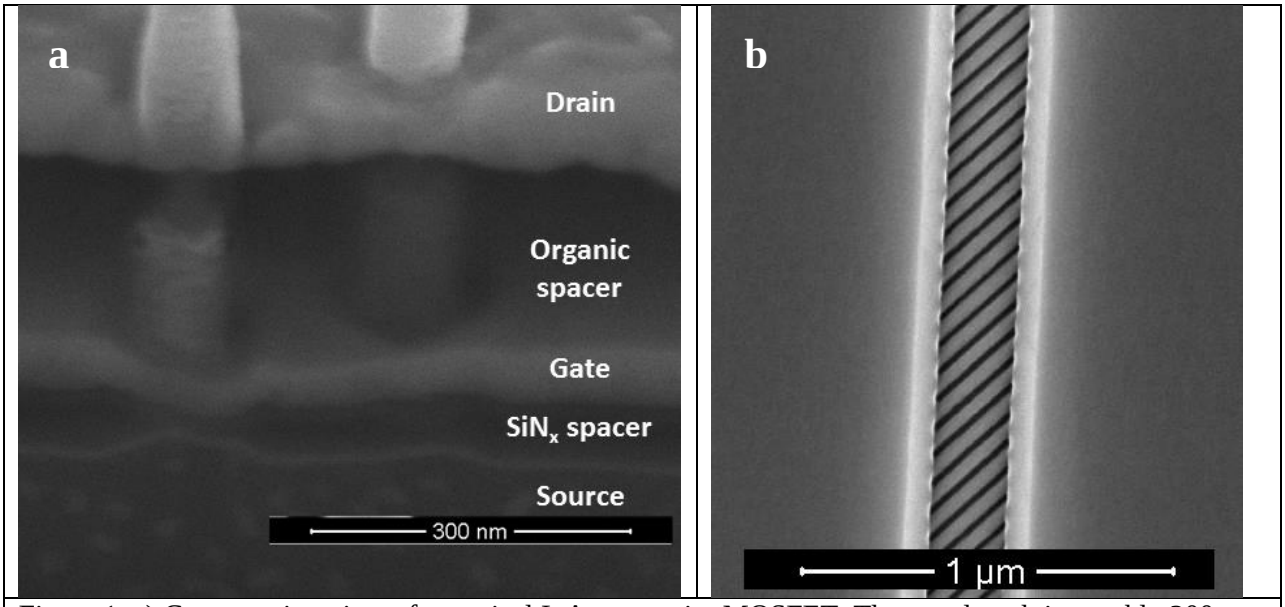

Figure 1. a) Cross section view of a vertical InAs nanowire MOSFET. The gate length is roughly 200 nm. b) Top view of lateral $In_{0.6}Ga_{0.4}As$ nanowires with n^+ regrown ohmic contacts.

The lateral InGaAs wires show a maximum g_m=1.67 mS/µm at V_{ds} 0.5V and g_m=1.8 mS/µm at V_{ds}=1.0V at L_g=32 nm. R_{on}=270 Ωµm. For a L_g=200nm, a sub thresholdslope SS=103 mV/decade at V_{ds}=0.5 and 83 mV/decade at 50 mV has been obtained. The self-aligned T-gate give low parasitic capacitances and gate resistance, yielding a maximum f_T=187 GHz and f_{max}=270 GHz.

Both the lateral and vertical fabrication scheme is highly scalable, and can be optimized for transistor gate lengths below L_g=20 nm.

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