Student Paper

Turn-on Transient Behavior of PD SOI NMOS Device Considering the Back-Gate Bias Effect

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SOI MOS devices may have notorious floating-body related kink effects due to buried oxide [1]. As for the bulk CMOS devices, the back-gate bias effect of the PD SOI NMOS devices may influence their DC behaviors, complicating the function of the parasitic bipolar device in thin film[2]. As a matter of fact, the back-gate bias may also affect the transient behavior of the PD SOI NMOS device. In this paper, the turn-on transient behavior of the PD SOI NMOS device considering the back-gate bias effect is described.

Fig. 1 shows the TEM cross section of the PD SOI NMOS device under study[3]. The thin film of the test device is 70nm, doped with a p-type doping density of $3x10^{18}cm^{-3}$ above a buried oxide of 145nm in thickness. The front gate oxide is 1.5nm. In the channel region, in addition to the 60nm channel under the gate, a 65nm LDD region doped with an n-type density of $10^{19}cm^{-3}$ under a sidewall spacer has been adopted. Experimental measurement and the 2D simulation of the test device have been used to carry out the study.

By imposing a step voltage from 0V to 2V with a rise time of 20ns on the gate of the PD SOI NMOS device biased at V_D=2V, Fig. 2 shows the drain current during the turn-on transient with the back-gate bias of 0V, -20V and +20V, based on the experimentally measured data and 2D simulation results. As shown in the figure, with V_{back} of -20V, the drain current is the smallest and with V_{back}=20V, it is the largest since the back channel is turned on and the parasitic bipolar device has been pushed upward in the thin film. As indicated in the figure, the 2D simulation results are well correlated to the experimentally measured data. Fig. 3 shows the equivalent circuit model of the PD NMOS device considering the back-gate bias effect. As shown in the figure, in addition to the top channel, due to the back-gate bias effect, the impact ionization current in the bottom channel above the buried oxide also contributes to the base current, which triggers the turn-on of the parasitic bipolar device in the thin film. Based on the numerical extraction techniques, Fig. 4 shows (a) the multiplication factor (M-1) and the current gain (β) of the parasitic bipolar device in the thin film; (b) the collector current I_C of the parasitic bipolar device, the channel current I_{CH}, and the impact ionization current I_i; (c) the displacement currents- dQ_D/dt, dQ_S/dt, $C_{DG}(dV_G/dt)$, and $C_{SG}(dV_G/dt)$, during the turn-on transient of the PD SOI NMOS device biased at V_D=2V with a step voltage from 0V to 2V imposed on the gate voltage with a rise time of 20ns for the back-gate bias of 0V, -20V and +20V, extracted from the 2D simulation results. As shown in the figures, M-1 decreases during the turn-on transient due to the decrease in the post-pinchoff region and the current gain increases. As shown in Fig. 4(a), during the turn-on transient at 9ns while the top channel is not fully turned on yet and the back channel plays an important role, the case with V_{back}=-20V indicates the largest M-1 due to the largest post-pinchoff regions as compared to the cases with V_{back}=0V and +20V, which is correlated to the impact ionization current I_i behavior as shown in Fig. 4(b). At the end of the input ramp-up period, the top channel is fully turned on and the bottom channel is not influential any more, thus the current gain is smallest for the case with V_{back}=20V due to the largest base current in the parasitic bipolar device resulting from the largest I_i in the thin film. As shown in Fig. 4(c), the displacement current during the transient through the gate oxide is negligible as compared to the drain current. Fig. 5 shows the 2D hole concentration contours in the thin film during the turn-on transient of the PD SOI NMOS device biased at V_D=2V at 9ns with a step voltage from 0V to 2V imposed on the gate voltage with a rise time of 20ns for V_{back} of 0V, -20V and +20V, based on the 2D simulation results. As shown in the figure, for the case with V_{back}=-20V, the hole density in the post-pinchoff region is the largest among three V_{back} cases, which indicates the strongest M-1 and I_i for the negative back-gate bias, showing the influence of the bottom channel during the transient at 9ns as confirmed in Figs. 4(a)&(b).

References

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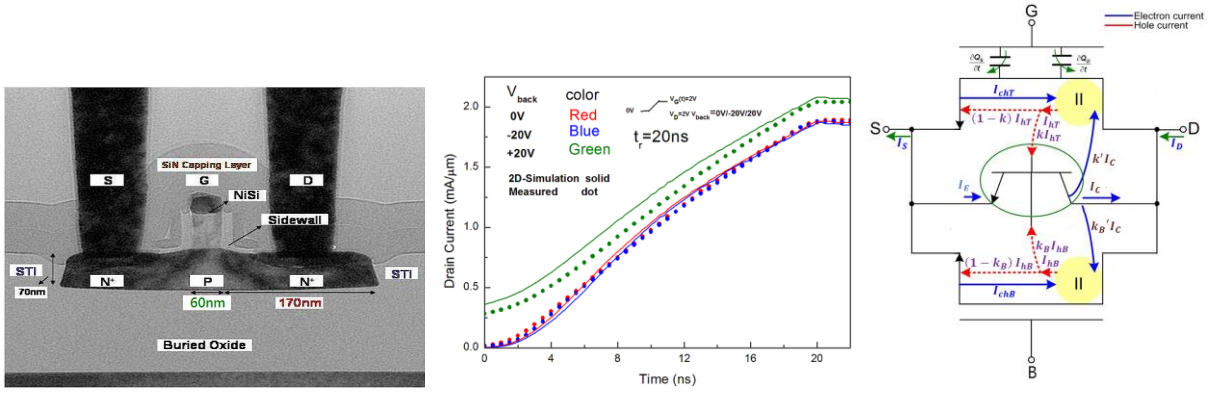

Fig. 1 TEM Cross section of the PD SOI NMOS device.

Fig. 2 Drain current of the PD SOI NMOS device biased at V_D=2V during the turn-on transient with a step voltage from 0V to 2V imposed on the gate voltage with a rise time of 20ns for the back gate bias of 0V, -20V and +20V, based on the experimentally measured data and 2D simulation results.

Fig. 3 Equivalent circuit model of the PD NMOS device considering the back-gate bias effect.

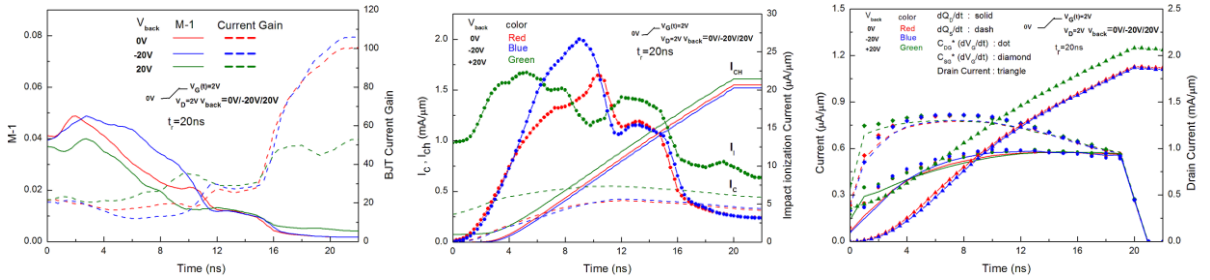

Fig. 4 (a) M-1 and current gain of the parasitic bipolar device; (b) Collector current I_C, channel current I_{CH}, and impact ionization current I_i; (c) dQ_D/dt, dQ_S/dt, $C_{DG}(dV_G/dt)$, and $C_{SG}(dV_G/dt)$, during the turn-on transient of the PD SOI NMOS device biased at V_D=2V during the transient with a step voltage from 0V to 2V imposed on the gate voltage with a rise time of 20ns for the back-gate bias of 0V, -20V and +20V, extracted from the 2D simulation results.

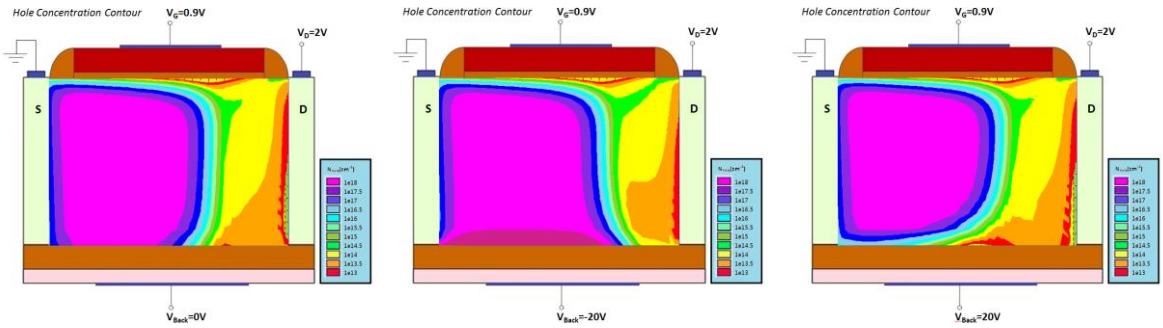

Fig. 5 2D hole concentration contours in the thin film during the turn-on transient of the PD SOI NMOS device biased at V_D=2V at 9ns with a step voltage from 0V to 2V imposed on the gate voltage with a rise time of 20ns for the back-gate bias of 0V, -20V and +20V, based on the 2D simulation results.