Student Paper

Base Current Degradation Mechanisms in NPN SiGe HBTs Subjected to High Current Stress

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As the scaling of semiconductor technology continues, modern SiGe HBTs are designed to operate at increasingly higher current densities, making the investigation of high current degradation mechanisms important. Under prolonged operation at high current densities, a device's performance can quickly degrade, commonly seen in the form of base and collector current drift with stress time [1-2]. Several mechanisms have been suggested as possible sources of such observed current shifts [3]. We identify a new mechanism for high current damage in SiGe HBTs that is associated with Auger generation.

We have stressed a series of NPN SiGe HBTs by applying simultaneous emitter current density J_E and collector-base voltage V_{CB} stress at temperatures of 300K and 373K, for a length of 10,000s, while periodically measuring the Gummel characteristics to track the evolution of the terminal currents resulting from stress. Under simultaneous application of high current density and low voltage stress, three degradation patterns are evident from the Gummel characteristics, as reported in other studies [1-2] and shown here in Fig. 1: 1) a rise in non-ideal base current at low base-emitter voltage ($V_{BE} < 0.6V$), 2) a decrease in the ideal base current at mid-V_{BE} values ($0.6V < V_{BE} < 0.9V$), and 3) an increase in both the collector and base currents at high V_{BE} values ($V_{BE} > 0.9V$).

The degradation pattern seen at low V_{BE} resembles that observed in mixed-mode stress (simultaneous application of high voltages and currents) and is caused by the formation of trap states along the emitter-base (EB) spacer and shallow trench isolation (STI) oxide interfaces due to hot carrier impingement [4]. In mixed-mode stress, hot carriers are generated by an avalanche generation process in the collector-base junction; however, due to the lack of large electric fields under high-current/low-voltage operation, avalanche multiplication is a less likely source of hot carriers because of low impact ionization rates. A more likely hot carrier source is Auger generation near the EB junction, which is prevalent at high carrier densities, as originally suggested in [3]. Further evidence for Auger generation as the source of hot carriers is given by a threshold behavior in the degradation of I_B of around 10 mA/μm^2. At these current densities, V_{BE} exceeds 1.0 V, and the EB junction potential barrier is almost eliminated, causing a dramatic increase in local carrier concentrations in the base, and thus Auger generation, in the base. Auger generation rates for emitter current densities of 1 mA/μm^2 and 10 mA/μm^2 obtained from a TCAD model are shown in Fig. 2 to illustrate this threshold behavior. Impact ionization rates are also shown in Fig. 2 to illustrate the disparity between the two hot carrier generation mechanisms. With the hot carriers being generated closer to the EB spacer, the chance of carriers undergoing energy-robbing phonon interactions is greatly decreased, thus increasing the probability that a hot carrier will create a trap. As shown in Fig. 3, the excess base current at low V_{BE} increases rapidly at current densities above 10 mA/μm^2. As temperature increases, we also see increased degradation at a single current level, as shown in Fig 4. This behavior is in contrast to the temperature dependence seen in mixed-mode stress, which has decreased degradation at high temperatures due to increased phonon activity. The proximity of the hot carrier generation to the oxide interfaces under high current stress diminishes the effect of this increased phonon activity, and the increase of the Auger generation rate with temperature [5] dominates the temperature dependence of the trap creation process. This temperature dependence has also been seen in MOSFET structures under similar stress conditions [6].

At current densities below 10 mA/μm^2, the current and temperature dependencies of the net trap creation rates are convoluted by the interplay of the Auger driven trap creation and an annealing process driven by hydrogen diffusion. As reported in [1], high current densities will release atomic hydrogen trapped in the poly-Si emitter and at the poly-Si/metal interface, which can then diffuse further into the emitter layer and passivate dangling bonds along the poly-Si grain boundaries and the poly-Si/crystalline-Si interface. This passivation will lower the recombination velocity at the poly-Si/crystalline-Si interface, leading to the decrease in the ideal base current, as we see in the mid-V_{BE} range. This dangling bond passivation also leads to a decrease in the emitter resistance R_E, which manifests as an increase in both I_C and I_B in the high-V_{BE} range. Both of these changes can be seen in Fig. 1. Increases in both stress current density and temperature will lead to an accelerated annealing process due to a larger amount of atomic hydrogen being freed and increased diffusion rates, respectively.

Unlike in mixed-mode stress degradation, which can be accurately modeled solely by hot carrier interactions, condensing the effects of high current stress into a single analytic form will require understanding of the interplay between multiple damage and annealing mechanisms.

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References

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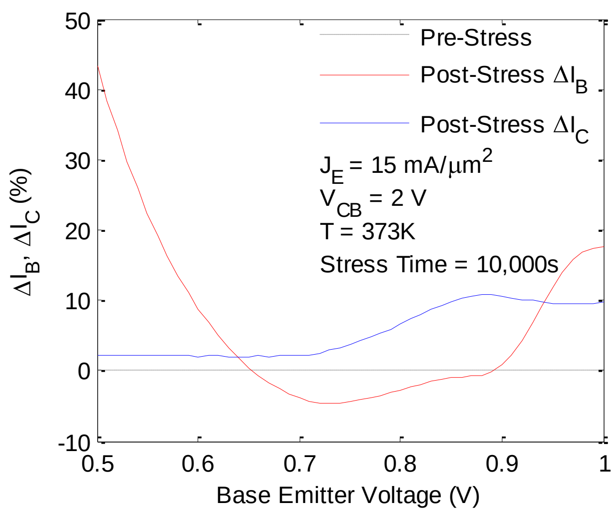

Fig. 1. Change in base current from the SiGe HBT Gummel characteristics after high current stress.

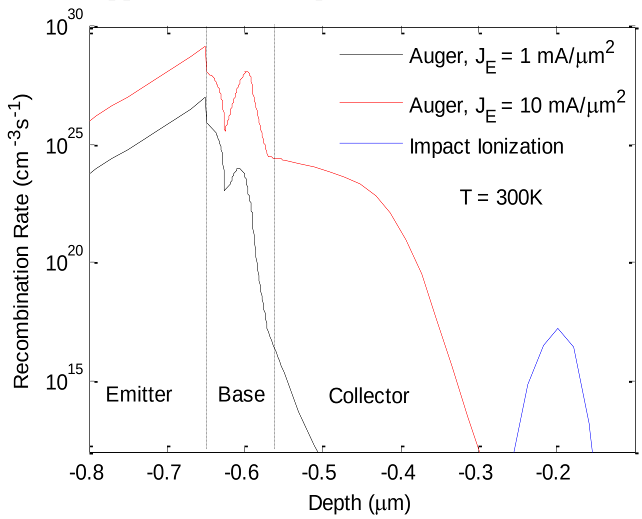

Fig. 2. Auger generation and impact ionization rate cross section at high current densities from TCAD.

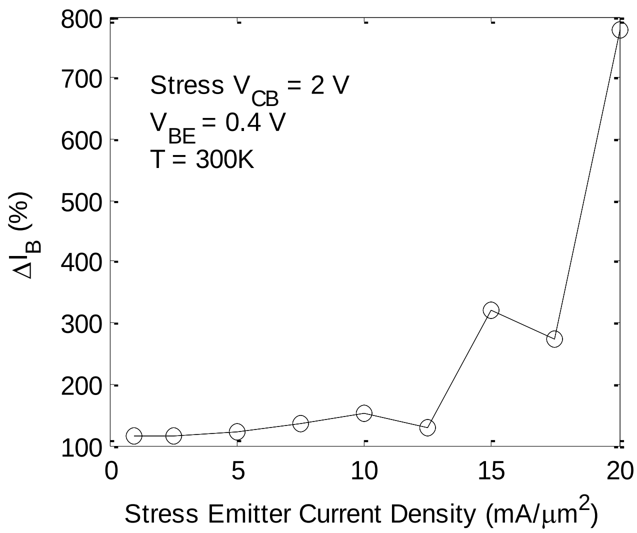

Fig. 3. Threshold behavior of base current degradation around 10mA/μm^2.

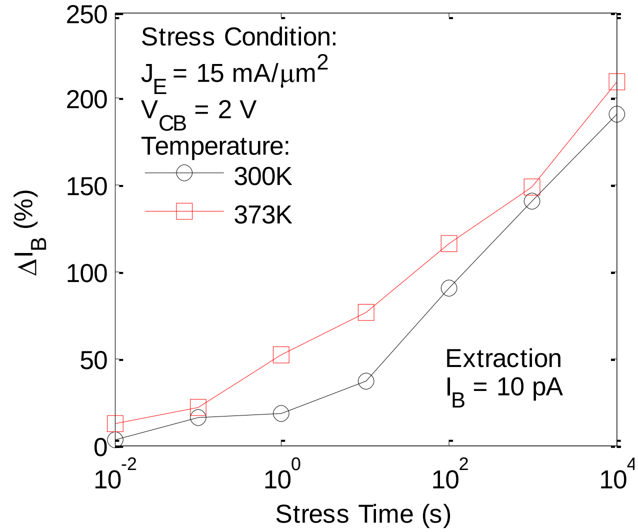

Fig. 4. Base current evolution at I_B = 10 pA for different temperatures under high current stress.