Student Paper

High speed Bias Temperature Instability measurements on sub-20 nm RMG HKMG MOSFETs

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The authors present a study of measuring threshold voltage (V_T) degradation through NBTI in p-channel MOSFETs fabricated using the sub-28 nm Poly/SiON and HKMG technology. The change in V_T during stress was calculated using the method outlined in [1]. Bias temperature instability occurs when the MOSFET is operated at high temperature and high gate voltage. It is due to two mechanisms: trapping of charge into charge-trapping defects in the oxide and generation of interface states (N_{it}) in the oxide during stress [2]. The former mechanism is reversible especially, in thin oxides due to de-trapping of trapped charge from the defect. This leads to recovery which starts immediately after the removal of stress. The recovery has been shown to display a log (t) dependence starting from a few μs [3]. Thus, the amount of time taken to sample the drain current (also called sense delay) plays a very crucial role and has to be kept as small as possible to ensure that both the charge trapping component and interface defect generation is monitored. The Agilent B1530A Waveform Generator/Fast Measurement Unit (WGFMU) was chosen for this study because it can sample with a resolution of 10 ns allowing us to acquire >50 samples of drain current within the targeted sense delay of 1 μs.

The WGFMUs are installed in the B1500A analyzer and are connected to Remote Sense and Switch Units (RSUs). A schematic of the High Speed BTI measurement is shown in Figure 1. The set up consists of Probe card/Probe tips, RSU units and B1500 with WGFMU's. The ideal setup recommended by Agilent for fast measurements is shown in Figure 2. We extended the capability to use a probe card instead of individual probe tips by modifying the grounding configuration for Source/substrate. With our approach we could use the conventional probe cards without the need for a more custom set up. The communication between the WGFMU port on the B1500A and the RSU is digital eliminating any concerns about signal distortion due to the cable length. On the other hand the cable length between the DUT under test and RSU needs to be optimized to reduce ringing and achieve steady state reading within 1 μs. The impact of cable length reduction from 3m to 1m is shown in Figure 3. The parasitic of the connection between the RSU and the probe card had to be negligible. A photograph of the final set up is shown in Figure 4.

Typically during BTI measurement stress-sense-stress (SMS) technique is used. During sense operation it is critical that the delay in the set up is kept ~1us with little to no impact on the signal integrity while switching from high stress voltage to a low sense voltage. To ensure a 1μs read out we observed that the compliance setting on the WGFMU is critical to discharge the gate-drain capacitor while the gate voltage switch from stress to the use condition and the drain switches from 0 to 50 mV. **Error! Reference source not found.** shows that for the devices we measured, a compliance of 100 μA on both the gate and the drain was required to settle the transients within 1 μs. For a lower compliance (10 μA), the settling time was approximately 2 μs. To obtain the final drain current during sensing, samples in the stable phase are averaged.

NBTI device degradation using the WGFMUS with 1us delay is compared to a measurement also done using WGFMU's but with 2ms in Figure 6. Clearly at short stress time more recovery is observed for the 2ms data and a higher time exponent is measured. As the stress progresses the 2ms and 1us data merge leading to almost no difference in EOL projection. But care needs to be taken to understand the impact of stress time interval used to estimate the time slope. Further work in this direction is under way and will be shared at the conference. To summarize, we have designed a setup to perform fast BTI degradation measurement in MOSFETs and achieved a minimum sense delay and sampling interval of 1 μs and 10 ns respectively. Currently, we are gathering more data on degradation of V_T with different stress voltages, durations and sense delays for determining the effect of these parameters on NBTI for the sub-28 nm technology.

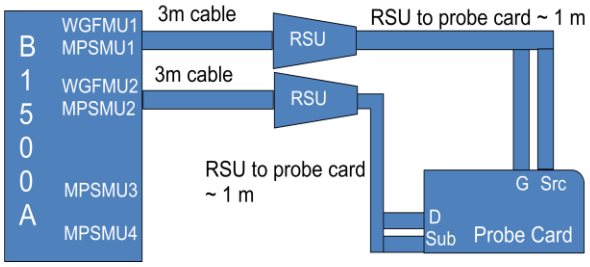

Figure 1: Schematic of the measurement setup (not to scale)

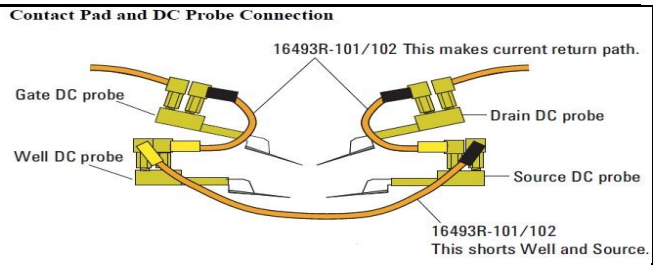

Figure 2: Measurement setup suggested by Agilent for fast measurements. [4]

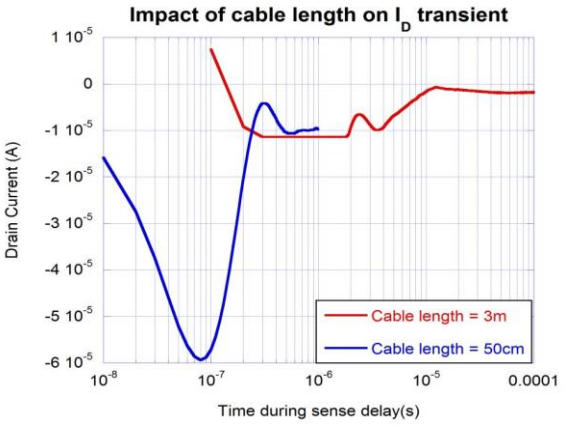

Figure 3: Impact of reducing the cable length from the RSU to the probe card.

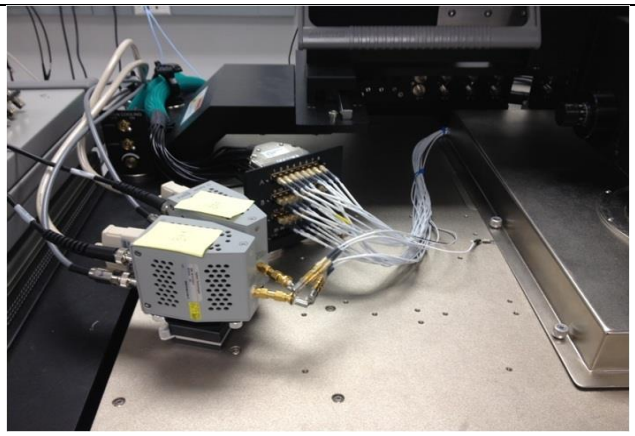

Figure 4: Photograph of the measurement setup.

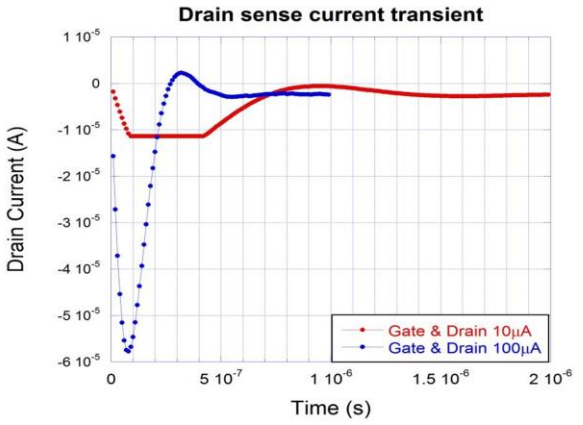

Figure 5: Impact of current compliance limit on settling time of the MOSFET.

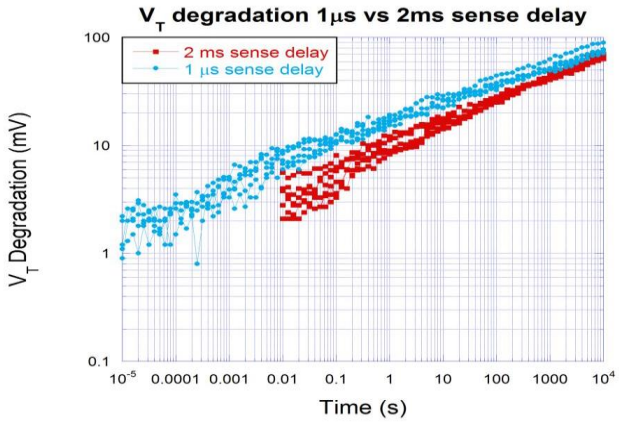

Figure 6: Impact of sense delay on V_T degradation.

References

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[3] M. Eshrov et al., "Dynamic recovery of negative bias temperature instability in p-type metal–oxide–semiconductor field-effect transistors," *Applied Physics Letters*, vol. 83, no. 8, p. 1647, August 2003.

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