Student Paper

A Novel Resistive-Gate Field-Effect Transistor with 24.7mV/dec Subthreshold Slope based on a Resistive TiN/TaO_x/Poly-Si Gate Stack

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In recent years, steep-slope devices of sub-60mV/dec with new operation mechanisms have been widely discussed, including tunneling FETs with quantum mechanical band-to-band tunneling mechanism [1], negative-capacitance FETs with ferroelectric gates [2], and Nano-Electro-Mechanical devices with movable gate or body [3]. In this paper, a new concept of steep-slope devices for ultra-low-power digital logic applications by utilizing the resistive switching of a metal-insulator-metal (MIM) gate stack, called Resistive-gate FET (ReFET), is proposed and experimentally demonstrated with steep subthreshold slope (SS) of 24.7mV/dec.

Fig. 1 shows the schematic structure of proposed ReFET with a MIM gate stack, in which the insulator is a kind of resistive switching material. As shown in Fig. 2, with the increased gate voltage, the voltage across the MIM structure increases and may induce an abrupt switching event from a high-resistance state (HRS) to a low-resistance state (LRS). This behavior may trigger a sudden increase of the surface potential of ReFET, resulting in an abrupt switching behavior with sub-60mV/dec SS.

In this work, n-type ReFETs based on a TiN/TaO_x/Poly-Si gate stack were fabricated. The fabrication process flow is shown in Fig. 3. After the deposition of TaO_x by RF reactive magnetron sputtering from a Ta target in the mixture of oxygen and argon ambient, an annealing process in the oxygen ambient was conducted to elevate the oxygen concentration of the TaO_x film. A stack of Pt/TiN/TaO_x/Poly-Si of 200nm/10nm/30nm/150nm was finally deposited on gate oxide, and the interfacial TiO_xN_y layer between TiN and TaO_x (Fig. 4) may act as an oxygen reservoir for switching. The internal voltage (V_{int}) on Poly-Si is also probed by designing the test structure of ReFET (Fig. 5) for further mechanism clarification.

As shown in Fig. 6, with floating V_G, measured I_D-V_{int} and I_D-V_{DS} curves of the MOSFET component of the fabricated ReFET both demonstrate good performance with a typical MOSFET behavior and the SS is about 70mV/dec at room temperature due to the limitation of kT/q.

On the other hand, by sweeping V_G with grounded V_{int}, the characteristics of Pt/TiN/TaO_x/Poly-Si stack of the fabricated ReFET are measured. As shown in Fig. 7, it exhibits a stable bipolar resistive switching behavior. The relatively low set voltage (<2V) with abrupt switching and large on-off ratio (>10^3) in the MIM gate stack is very beneficial to steep SS, low V_{DD} and large on-off ratio for ReFET. In the Pt/TiN/TaO_x/Poly-Si structure of this work, the migration of oxygen ions or vacancies under the electric field in TaO_x may result in the formation and rupture of oxygen-vacancy conducting filament, and may be responsible for the abrupt switching behavior. In addition, as shown in Fig. 8(a), I-V characteristics of current conduction in the HRS fit well with Schottky emission model $(ln(I) \sim V^{1/2})$, and the linear relationship in the LRS (Fig. 8(b)) shows the ohmic conduction. By using the MIM structure with threshold-switching materials [4], the operation of ReFET can be further optimized.

Fig. 9 shows measured transfer characteristics of the proposed ReFET in this work. It can obtain ultra-steep switching behavior of 24.7mV/dec SS, demonstrating its great potential for future low-power logic applications. However, the I_{ON}/I_{OFF} ratio is a little inferior which may be due to the high leakage current of MOSFET component at V_{int}=0V (Fig. 6(a)), and it can be improved by optimizing the gate work function. Moreover, the operation voltage of ReFET also can be further reduced by optimizing the switching voltage of the MIM stack.

References

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[4] M. Son *et al.*, “Self-Selective Characteristics of Nanoscale VO_x Devices for High-Density ReRAM Applications,” *IEEE Electron Device Lett.*, vol. 33, no. 5, pp. 718, May 2012.

Acknowledgements

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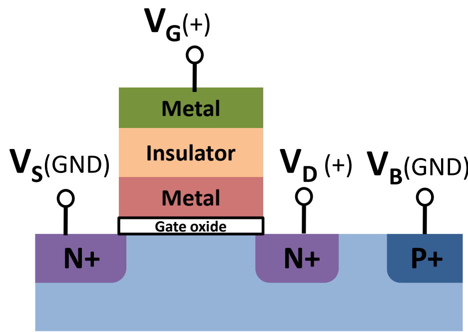


Fig.1 Schematic structure of proposed n-type ReFET with MIM gate stack.

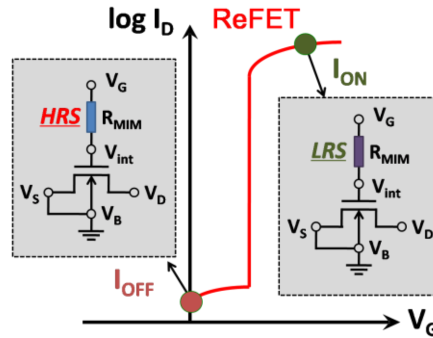


Fig.2 Illustration of the principle of ReFET with abrupt switching.

Isolation
Gate oxide, SiO_2 5nm
Poly Si deposition & patterning
Source and Drain: *N+ As implant (50keV, 4×10^{15}cm^{-2})*
Bulk: *P+ BF_2 implant (40keV, 5×10^{14}cm^{-2})*
RTA 1050℃ 10s
Lithography & Mask formation
PVD TaO_X
Anneal in O_2 under 400℃
Lithography & Etching
PVD TiN/Pt 10nm/200nm
Lift-off

Fig.3 Process flow of the n-type ReFET in this work.

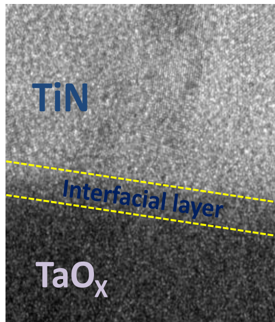


Fig.4 Cross-sectional TEM image of the interface between TiN and TaO_x.

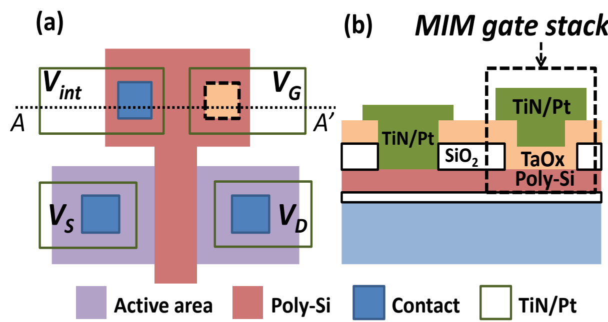
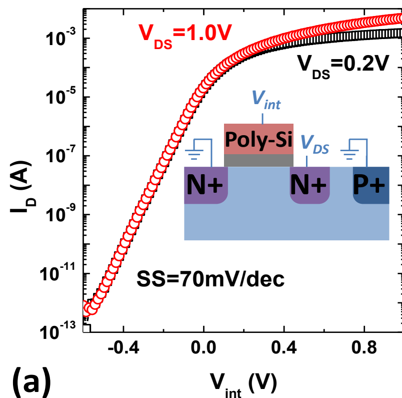


Fig.5 (a) Schematic top view of the test structure of ReFET in this work. (b) Cross section of ReFET along AA' in (a).



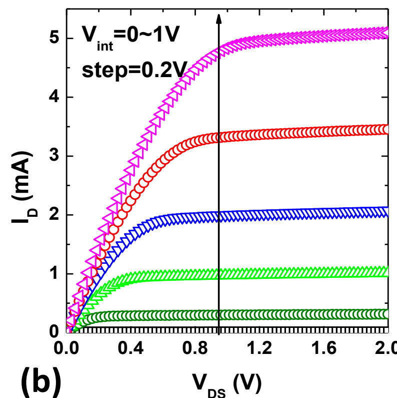


Fig.6 Measured (a) transfer and (b) output curves of MOSFET component in the fabricated ReFET. (W/L=160μm/5μm)

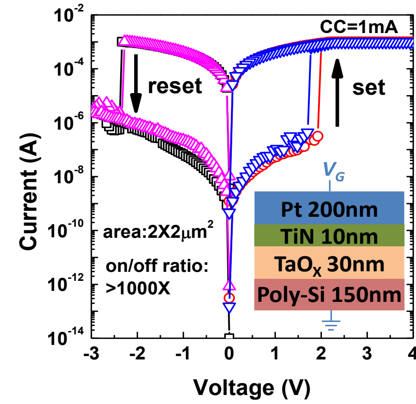
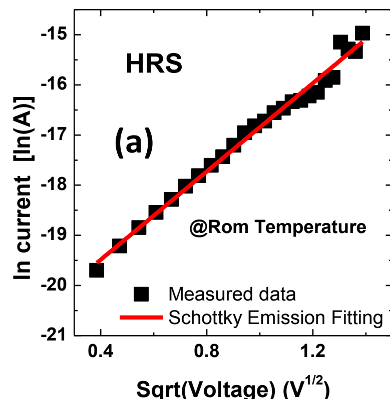


Fig.7 Measured I-V curves of MIM structure in the fabricated ReFET.



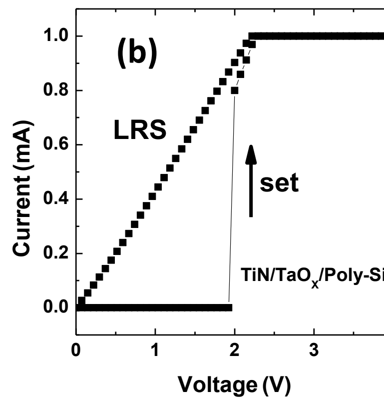


Fig.8 (a) I-V characteristics of Pt/TiN/TaO_x/Poly-Si in the HRS fit well with Schottky emission model. (b) shows a linear relationship in the LRS.

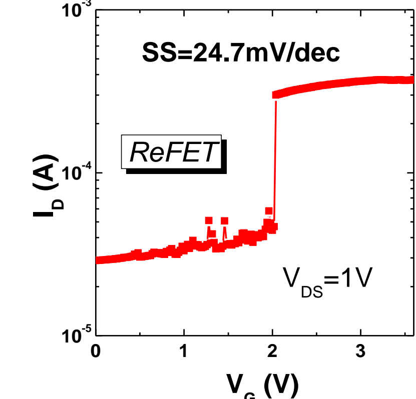


Fig.9 Measured I-V curves of the fabricated ReFET.