A Simple Analytical Variable Barrier Transistor Drain Current Model Matched Against Experimental Data

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Abstract

In this paper we present, a simple analytical model for the computation of the drain current in a new type of transistor, a VBT (Variable Barrier Transistor).A good agreement between our results and experimental data, proves the accuracy of this model. The experimental data show that the Ion/Ioff ratio of this device can be improved and our model reproduces these results.

Introduction

To fully benefit from scaling at nowadays level, new device architectures are needed. The variable barrier transistor (VBT) device is one of those and it is able to achieve sub-*kT /q* subthreshold slope using intra-band tunnelling through constriction barriers [1]. The constrictions result in the formation of energy barriers that can be used to improve the on/off current ratio and switching characteristics of transistors. In a VBT the barrier height is V_{GS} dependent. By placing a barrier such as a constriction at the edges of the gate, the natural movement of the energy bands with V_{GS} can be used to improve the control of the transparency of the barrier in such a way that the off-current is blocked more efficiently than the on-current.

Device modelling

We consider an undoped nanowire MOSFET, with two constrictions at the end of the channel (See Fig.1(a)). The intrinsic height of the barrier in the constriction can be adjusted by modifying the thickness of the constriction.(Δtsi). Then, the resulting barrier is:

$$\Delta E = E_1(t_{Si} - \Delta t_{Si}, W_{Si} - \Delta W_{Si}) - E_1(t_{Si}, W_{Si}) \quad (1)$$

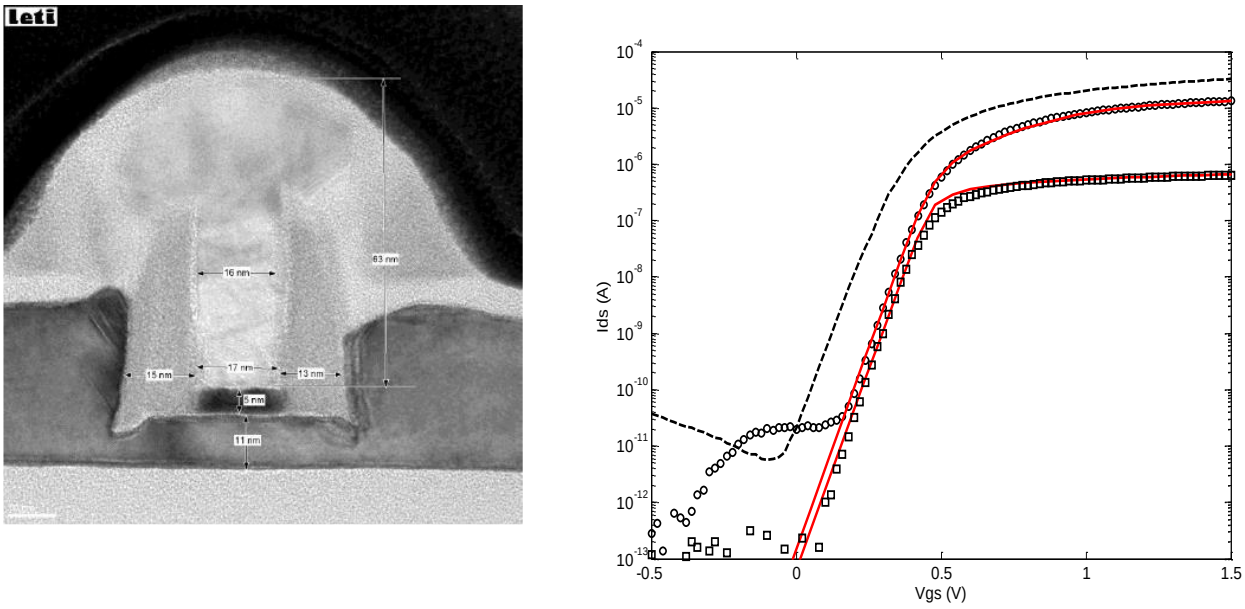
where W_{Si} and t_{Si} are the transistor width and thickness, while ΔW_{Si}(=0.2nm) and Δt_{Si} (=0.2nm) are the variation of width and thickness in the constriction, respectively. E_1 can be described quite well by the effective mass approximation (parabolic *E-k* dispersion relationship). The intrinsic barrier is further modulated by the gate voltage induced electric field, in this case the fringing electrostatic field near the gate edges and therefore, the top of the barrier decreases linearly with V_{GS} , so it will be higher in subthreshold regime and lower in the above threshold regime. [2].The barrier height is computed as follows:

$$BH = -\left(\Delta E / q - \alpha\left(V_{GS} + \Delta V_{GS}\right) + \beta V_{DS}\right) \quad (2)$$

where α and β are fitting parameters. Choosing their value is very important, especially when dealing with experimental data. In our case α=0.85 (used for adjusting the subthreshold slope) and β=0.98 (used for accounting for the DIBL-like effect present in the experiments) ΔV_{GS} is a correction factor of the gate voltage of 0.17V. Having the barrier height, the current can be computed. The drain current in subthreshold regime, considered a thermionic current, is computed using the Landauer theory where the current through a conductor is expressed in terms of the probability that an electron can transmit through it. The length of the constriction (or the barrier width) is a very important parameter to consider, because it establishes if the dominant conduction mechanism through it is tunnelling or thermionic current. It should be kept in the range of 1-4nm in order to have a high probability of electron tunnelling through the barriers. In the devices we studied the length of the constriction was longer, and therefore the dominant subthreshold mechanism was thermionic emission. [3]. However, until now, the fabrication of the constrictions can only get to 13nm. In this case the tunnelling current becomes negligible and the thermionic one will be the dominant one in subthreshold regime.

In this case the subthreshold thermionic current is:

$$I = -\frac{qkT}{\pi\hbar} g \cdot \ln\left(\frac{1 + e^{\frac{BH - E_{FS}}{kT/q}}}{1 + e^{\frac{BH - E_{FD}}{kT/q}}}\right) \quad (3)$$



(a) (b)

Figure 1. (a) Example of an experimental VBT. (b)Dotted line- The drain current of the same-dimensions transistor as the VBT with no constrictions for V_{DS}=0.9V. Straight line- our VBT model. Circles- experimental VBT drain-current for V_{DS}=0.9V. Squares- experimental VBT drain-current for V_{DS}=0.04V. The silicon nanowire has a channel length of L=21nm, channel width W=15nm, oxide thickness Tox=1.31nm, Si thickness Tsi=10nm (for the SRG model used for the above threshold region, the radius R=Tsi/2)

For the above threshold current, we used a drift-diffusion current model (I_{DD}) for a surrounding gate (SRG) MOSFET .We have combined the two current components using an interpolation function, in order to obtain the total current:

$$I_{DS} = \frac{I_{DD} I}{I_{DD} + I} \tag{4}$$

If we make a comparison between the Ion/Ioff ratio for a transistor Fig1(b)) with no constrictions and the VBT we can see that the Ion/Ioff ratio of the VBT is higher, thus improving the switching characteristics of the transistor with V_{GS}. This demonstrates that even with a long constriction, VBT devices exhibit one important advantage over devices with no constrictions

Ion/Ioff of the transistor with no constrictions=8.07X10^5
Ion/Ioff of the VBT =6.9X10^6

Conclusions

This paper is meant to be an explanation of the behaviour found in this particular experimental VBT and also a first attempt to model its drain current. Also, we are the first to map it against experimental data. The previously published papers that deal with the description of this device use only simulations. We consider it important that our model gives such a good agreement with the experimental data that show us an improved Ion/Ioff ratio of the VBT as compared to the standard no constriction transistor, making the VBT an important candidate for circuit implementation, but taking into consideration the need of various enhancements in the future. (like using a shorter constriction length, etc)

References

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