ISDRS 2013, December 11-13. 2013

Monolithic Integration of Laser Crystallized Silicon Devices for 3DIC

Vincent W. Lee[a], Alexander B. Limanov[b], Asit Ray[c], Robert Laibowitz[a], Hsiang-Lan Lung[d], Chung Lam[c], James S. Im[b], Ioannis Kymissis[a*]

[a] *Dept. of Electrical Engineering, Columbia University, USA, johnkym@ee.columbia.edu,* [b] *Dept. of Applied Physics and Applied Math, Columbia University, USA,* [c] *IBM T. J. Watson Research Center, USA,* [d] *Macronix Int. Co., Taiwan*

Introduction: Scaling of conventional CMOS circuits becomes increasingly expensive and difficult as devices are pushed towards fundamental physical limits. As this limit is approached, three dimensional integrated circuits (3DIC) are being explored as a way to augment the functionality of traditional CMOS devices. 3DICs are currently being explored through two methods: bonding using Through Silicon Vias (TSV) [1][2] or monolithic integration of thin film transistors using various materials, such as, solid phase epitaxial silicon [3], or oxide semiconductors [4]. Bump bonding with TSVs can offer high quality CMOS devices, but also increases costs and complexity by requiring a second CMOS chip and processes such as wafer thinning and alignment. 3DICs built monolithically can be more cost effective, but require high performance devices and processes compatible with back-end-of-line tolerances. Presented here are two fully monolithic device processes which are compatible with BEOL tolerances and offer high levels of performance. Additionally, in the context of 3DICs, front-end transistors processed with and without laser processing are compared to directly determine the effects of the laser irradiation on the front-end.

Lateral Transistors: Lateral devices begin with an electron beam deposition of 1µm of SiO_2 and 100nm of Si. The deposition chamber has a base pressure of 10^{-7} torr to ensure low gas incorporation and the substrate is held at 400°C during deposition to improve film quality. Next, line-scan sequential lateral solidification (SLS) laser processing is performed with a 308nm XeCl excimer laser, fig. 1a. SLS is a complete melt laser crystallization process which combines the high energy laser pulse with micro-translations of the sample stage. More information on the line-scan SLS process can be found in Sposili, et al. [5]. The remainder of the processing steps include ion implantation, dopant activation with either RTA or laser annealing methods, active area etch, aluminum-silicon source/drain electrodes, Parylene-C gate dielectric, and aluminum gate metal. Fig. 1 shows IV characteristics of transistors with grain boundaries parallel to current conduction, and a micrograph of completed devices.

These transistors exhibit high mobilities along the polycrystalline grain boundaries of 450 cm^2/Vs and

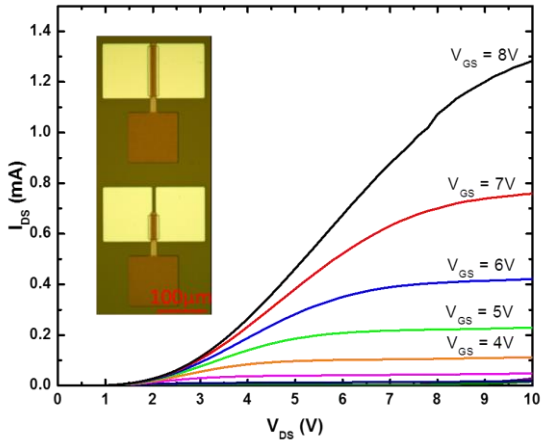


Figure 1: SLS transistors with grain boundaries parallel to current conduction. W/L=100/20, µ~450 cm^2/Vs, V_T~1.7 V. Inset shows micrograph of completed laser crystallized transistors.

250 cm^2/Vs perpendicular to the polycrystalline grain boundaries and agree with other devices made using similar methods in literature [6]. The high contact resistance can be resolved through a higher implant dose and switching the RTA process to a non-melt laser anneal which also provides process compatibility with low temperature substrates required for 3DIC integration concepts. A 2-3X improvement in sheet resistance of the doped silicon contacts is observed with these process changes measured by the van der Pauw method.

Vertical Diodes: A second type of device is fabricated in a vertical format. The vertical column of amorphous silicon and the overburden is irradiated with a single laser shot. The laser beam is shaped through projection optics and a quartz photomask with a 1 mm x 1 mm exposure area. A high precision stage stitches together individual 1 mm x 1 mm squares to cover the entire wafer. Like previous transistors, the combination of short pulse durations, limited exposure areas, and silicon dioxide buffer allows for the full melt of the amorphous silicon while keeping the front-end devices at low temperatures.

The laser energy density is adjusted to melt the entire vertical column of amorphous silicon. Nucleation begins at the bottom of the vertical column and is seeded by the underlying single crystal silicon substrate. Amorphous silicon crystallization was studied with SEM and TEM, and TEM electron

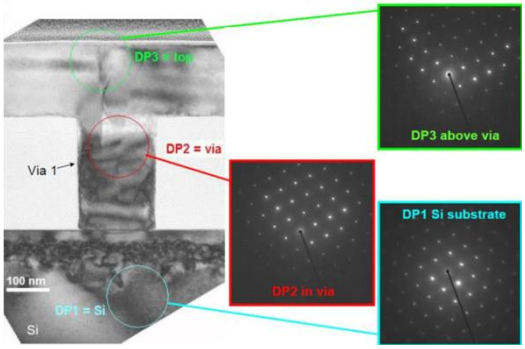


Figure 2: Bright field TEM image and electron diffraction images showing each region with high degree of crystallinity and having the same crystal orientation as the silicon wafer.

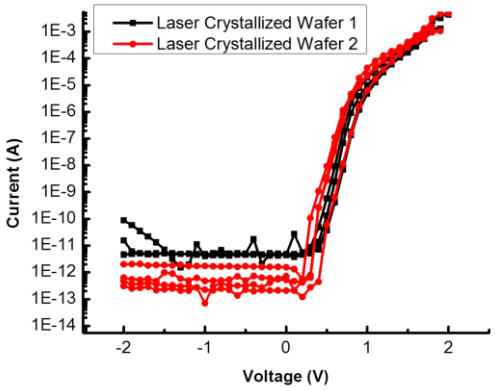
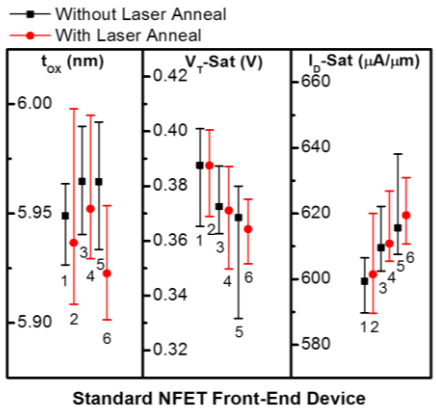


Figure 3: IV characteristics of laser crystallized diodes. Squares and circles show multiple devices on two wafers.



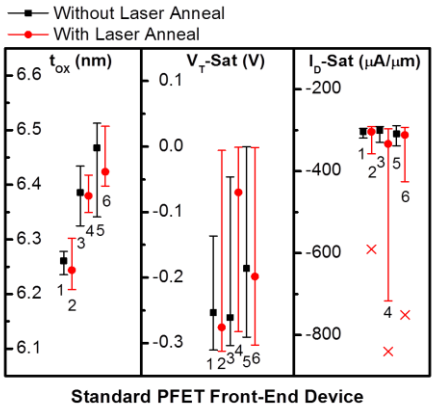


Figure 4: Front-end transistor parameters (t_{ox}, V_T-Sat, I_D-Sat) for NFET and PFET devices. Each line plots the maximum, minimum, and median of twenty measurements. Overall, except for possible processing issues in p-channel wafer 4, the laser crystallization process does not have any measurable effect on front-end characteristics.

diffraction studies show all three regions (single crystal wafer, vertical column, and solidified overburden) have the same crystal orientation, fig. 2.

Vertical diode devices are then fabricated by performing a silicon etch-back, ion implanting p-type dopants for ohmic contact, dopant activation, and deposition and CMP of tungsten contact electrodes. IV characteristics are plotted in fig. 3. The designed mask measures two diodes in parallel. IV characteristics of laser crystallized diodes show consistent behavior across multiple wafers and multiple devices. In addition, the high possible current densities (up to $3.05*10^7$ A/cm^2) point to high quality material within the vertical structure. Similar vertical geometry epitaxial diodes fabricated with higher thermal budget processes show comparable current densities.

Front-End Characterization: For 3DIC concepts, the described laser crystallization processes must offer low enough process temperatures to not affect front-end transistor behavior. Fabricating fully functional front-end transistors prior to laser processing offers the most direct method of characterizing the effects of laser irradiation. Six wafers are prepared, three with the laser crystallization process, three without, following the process for fabricating vertical column diodes. Twenty n-channel and twenty p-channel transistors are measured across each wafer, and t_{ox}, V_T-Sat, and I_D-Sat parameters are extracted and tracked. Fig. 4 shows these parameters; each of the lines represents the range of all twenty measured transistors, marking the median and two end points. Overall, the laser crystallization process has no effect on front-end characteristics. This is a direct validation that laser crystallization processes are compatible for adding active layers above standard CMOS transistors.

Conclusion: To commercialize monolithically integrated 3DICs, a method of fabricating high quality devices directly on conventional CMOS is required. Presented here are two such laser crystallized devices, lateral transistors and vertical diodes, paving the way for new architectures and designs, where devices with different functions or size constraints can be placed on the back-end without disturbing conventional front-end devices.

References:

[1] M. G. Farooq, et al. IEDM, pg. 7.1.1, 2011.
[2] D. Y. Chen, et al. IEDM, pg. 14.3.1, 2009.
[3] P. Batude, et al. IEDM, pg. 7.3.1, 2011.
[4] K. Kaneko, et al. IEDM pg. 7.4.1, 2011.
[5] R. Sposili, et al. APL 69 (19), 1996.
[6] Y. H. Jung, et al. MRS Proc. 621, pg. Q9.14.1, 2000.