Student Paper

RIE Induced Roughness and Inversion Mobility on SiC

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The need for high power, high temperature energy saving electronics, has led to a renewed interest in SiC based MOSFET type devices. Enhancements in the basic crystal quality and interface passivation suggest that such a SiC MOS based technology can be realized. The trench MOSFET is a desirable configuration given its higher current density than DMOSFET. Beginning with the Si-face surface of SiC , trench side walls correspond to a-faces, including the (11-20) face that displays the highest mobility of any common SiC-4H face (e.g. 85 cm^2/V-s with a NO POA on epi material **Error! Reference source not found.**, compared to 45cm^2/V-s on Si-face). However a practical trench MOSFET formed via a Reactive Ion Etch (RIE) is not satisfactory, mainly due to poor MOS channel mobility **Error! Reference source not found.**. RIE introduces roughness to both the bottom and side wall of the trench. A hydrogen based etch process is known to substantially reduce such roughness **Error! Reference source not found.**.

In this study, on a-face 4H-SiC material, we trace the evolution of MOSFET channel mobilities from epi ready to RIE and H etch recovery in Fig.1 and 2, and correlate the mobility to its surface roughness at each step in Fig. 3. A strong and monotonic correlation between surface roughness and mobility reduction is observed. RIE induced surface roughness is found to be the mobility limiting factor and H etch is proven effective in roughness and mobility recovery. Power Spectral Densities method is used to compare AFM data in Fig.4 and table 1, and mobility limiting mechanisms are discussed and compared to past work in SiC and Si.

References

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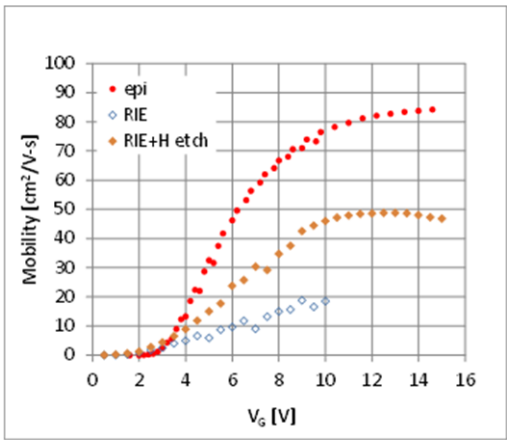

Fig.1. Field effect mobilities with a 2h standard NO anneal, beginning with peak μ=85 cm^2/Vs with epi , then reduced to μ=20cm^2/Vs after RIE roughening and recovered to at least μ=50cm^2/Vs after H etch (under-estimated).

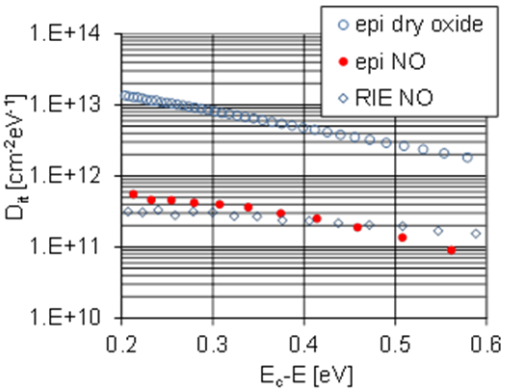

Fig.2. Interface Trap Density (D_{it}) vs energy level 0.2 to 0.6 eV below conduction band, extracted from Hi-Low C-V measurements on companion n-type MOSCAP's. Empty circles are unpassivated, stars and filled circles are epi and RIE with NO anneal at 1175°C 2hr, respectively. RIE+H etch sample NO anneal D_{it} is identical to that of epi NO.

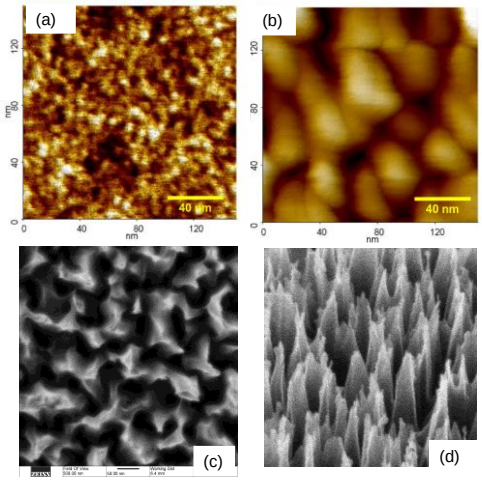

Fig.3. (a) and (b) are AFM surface images of 'epi' and 'RIE'(70nm SiC etched) surfaces, taken after MOSFET mobility evaluation and gate oxide removal by HF. The height scales are ±0.4nm in (a) and ±20nm in (b). The corresponding RMS values are 0.095nm and 5.527nm respectively, scan area is 140^2 nm^2. (c) and (d) are Helium Ion Microscope top view and 45°side view images of sample surface immediately after RIE process that removed 350nm SiC and before any additional treatment. The scan area is 500^2 nm^2. After a 1400°C 5min H_2 etch process, the surfaces of (b) is recovered epi-like quality as in (a).

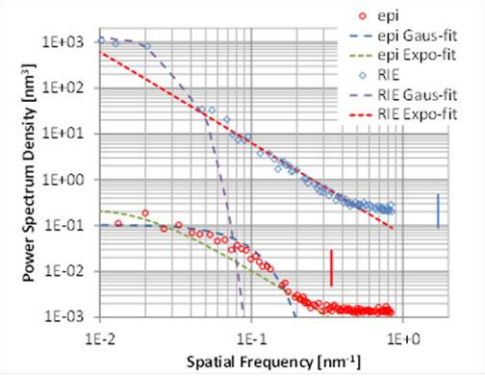

Fig.4. Power Spectral Densities from AFM profiles of 'epi' and 'RIE' in red circles and blue Diamonds. The corresponding fittings with Gaussian and Exponential autocorrelation function are in dash and dot lines. Mean free paths of each case calculated from corresponding mobilities are marked by straight lines (same color code).

Table1 peak field effect mobilities from electrical test, the RMS step height Δ and the correlation length Λ from Gaussian or Exponential auto-covariance function fitting to PSD.

Surface Condition	Peak Mobility [cm^2/Vs]	Mean Free Path from mobility λ_m [nm]	Gaussian Fit [nm]			Exponential Fit		
			Δ [nm]	Λ [nm]	$(\Delta*\Lambda)^2$ [nm^4]	Δ [nm]	Λ [nm]	$(\Delta*\Lambda)^2$ [nm^4]
a-face epi	85	2.89	0.13	22	8.18	0.13	50	42.25
a-face RIE	20	0.58	8	85	4.6E5	10	500	2.5E7