Student Paper

Gate Leakage Current Suppression and Reliability Improvement for Ultra-Low EOT Ge MOS Devices by Suitable HfON/HfAlO thickness and Sintering Temperature

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Abstract—Ultra-low effective oxide thickness (EOT) Ge MOS devices with different HfON/HfAlO stacks and sintering temperatures were investigated in this work. Both the reduced gate leakage current and reliability improvement can be achieved by either a suitable gate dielectric stack or sintering temperature. As a whole, a 0.5 nm thick HfAlO in gate dielectric stack and a sintering temperature at 350 ^{o}C are the suitable conditions for ultra-low EOT Ge MOS devices.

Introduction: Since high-k gate dielectric has been implemented in metal-oxide-semiconductor field effect transistors (MOSFETs) and it generally results in mobility degradation, devices with higher carrier mobility are desirable to improve the performance of CMOS circuits. Ge has been regarded as the most promising material for improving the CMOS performance [1]. The quality of the interfacial layer (IL) between the gate dielectric and Ge substrate is very important for Ge devices [2]. Besides, the increase of the gate leakage current and the reliability degradation are the two key issues while device scaling down [2]. In this work, Ge MOS devices with different HfON/HfAlO gate stacks and sintering temperatures are studied.

Experiment: The fabrication processes of Ge MOS devices were started on an n-type Ge substrate (~5 ohm-cm). After HF clean, GeO_2 interfacial layer (IL) was grown by using H_2O plasma process within an atomic layer deposition system (ALD). Then, various thickness stacks of HfON/HfAlO gate dielectrics were in-situ deposited by the ALD, and followed by the deposition of 30 nm TaN with a sputtering. After metallization, lithography and gate etching processes, sintering process was performed on devices at different temperatures. The detailed split conditions are shown in Table. 1. Fig. 1 shows the process flow and the schematic cross-section of the Ge MOS devices in this work. All the stress conditions for reliability tests were performed at 3.3 MV/cm.

Results and Discussion: Fig. 2 and 3 show the CV curves and leakage current densities, respectively, of Ge MOS devices with different HfON/HfAlO stacks. The results indicate that both the capacitance and leakage current density decrease with increasing the thickness of HfAlO layer in HfON/HfAlO stacks. The cumulative probabilities of leakage current density for devices with different gate stacks are shown in Fig. 4, indicating that the uniformity is improved for samples with HfAlO layer. Fig. 5 shows the gate leakage currents at $V_g = V_{FB} +1$ V vs EOT of Ge MOS devices with some benchmarks for comparison. Fig. 6 and 7 show the stress-induced V_{FB} shifts and gate leakage currents, respectively, of devices with different HfON/HfAlO stacks. It is found that sample with a 0.5 nm thick HfAlO in gate dielectric stack shows the best reliability characteristics. Fig. 8 and 9 show the CV curves and leakage current densities, respectively, of the HfON gated Ge MOS devices with different sintering temperatures. The results indicate that both the capacitance and leakage current decrease with lowering the sintering temperature. Fig. 10 shows the gate leakage currents at $V_g = V_{FB} +1$ V vs EOT of HfON gated Ge MOS devices with different sintering temperatures. It is seen that sample with a sintering temperature at 350 ^{o}C is below the general trend line. Fig. 11 and 12 show the stress-induced V_{FB} shifts and gate leakage currents, respectively, of HfON gated Ge MOS devices with different sintering temperatures. Thus, the reliability characteristics of high-k gate dielectric can be improved by a lower sintering temperature.

Conclusions: The gate leakage current suppression and reliability improvement for ultra-low EOT Ge MOS devices can be achieved by a suitable HfON/HfAlO dielectric stack or sintering temperature. The optimal conditions in this work are a 0.5 nm thick HfAlO in gate dielectric stack and a sintering temperature at 350 ^{o}C.

References

[1] P. Zimmerman et al., “High performance Ge pMOS devices using a Si-compatible process flow” *IEDM*, p.1-4, 2006. [2] R. Zhang et al., ” High Mobility Ge pMOSFETs with 0.7 nm Ultrathin EOT using $HfO_2/Al_2O_3/GeO_x$/Ge Gate Stacks Fabricated by Plasma Post Oxidation” in *VLSI Symp. Tech. Dig.*, p.161, 2012.

Table. 1 Split conditions of devices with different HfON/HfAlO2 stacks and different sintering temperatures.

Device ID	Control	S1	S2	S3	300	350
Metal gate	TaN 30 nm				TaN 30 nm	
Gate dielectric	HfON 3 nm	$HfAlO_2$ 0.5 nm HfON 2.5 nm	$HfAlO_2$ 1 nm HfON 2 nm	$HfAlO_2$ 1.5 nm HfON 1.5 nm	HfON 3 nm	
Interfacial layer	GeO_2 (by H_2O plasma)				GeO_2 (by H_2O plasma)	
Substrate	N-type Ge substrate				N-type Ge substrate	
Temp. of sintering	400 °C				300 °C	350 °C

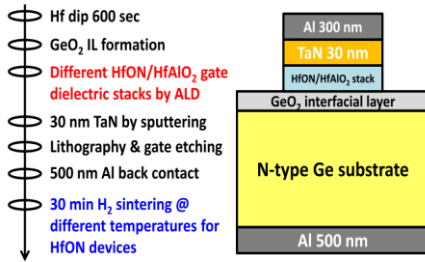

Fig. 1 Fabrication processes and schematic cross-section of devices.

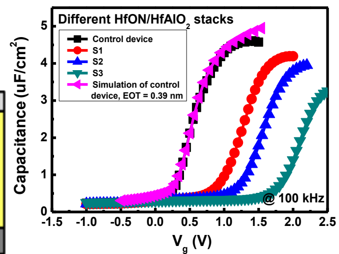

Fig. 2 CV curves of Ge MOS devices with different HfON/HfAlO stacks.

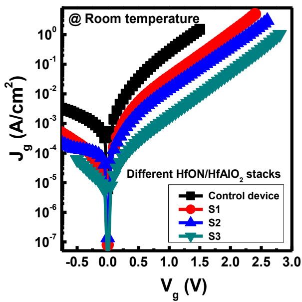

Fig. 3 Leakage current densities of Ge MOS devices with different HfON/HfAlO stacks.

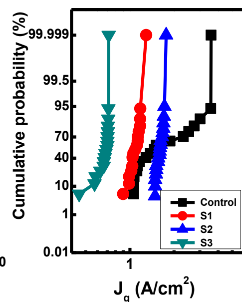

Fig. 4 Cumulative probabilities of leakage current density for devices with different HfON/HfAlO stacks.

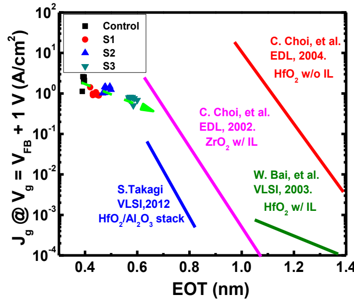

Fig. 5 Gate leakage currents at $V_g = V_{FB} + 1$ V vs EOT of n-Ge MOS devices with some benchmarks for comparison.

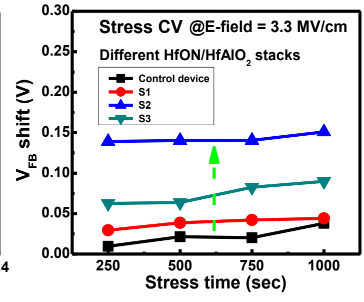

Fig. 6 Stress-induced V_{FB} shifts of Ge MOS devices with different HfON/HfAlO stacks, indicating the increase of the V_{FB} shifts.

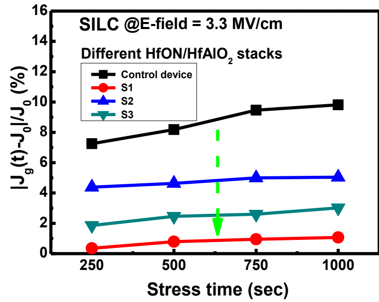

Fig. 7 Stress-induced leakage currents of Ge MOS devices with different HfON/HfAlO stacks, indicating the improvement of the interface quality.

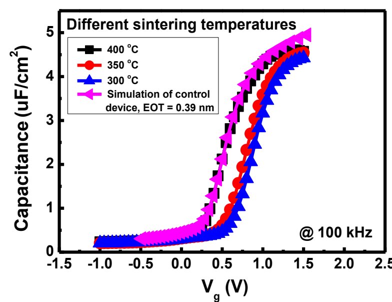

Fig. 8 CV curves of Ge MOS devices with HfON dielectrics after different sintering temperatures.

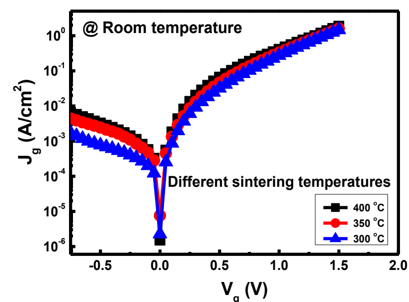

Fig. 9 Gate leakage current densities of Ge MOS devices with HfON dielectrics after different sintering temperatures .

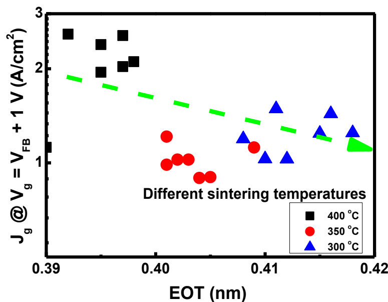

Fig. 10 Gate leakage currents at $V_g = V_{FB} + 1$ V vs EOT of HfON gated Ge MOS devices with different sintering temperatures.

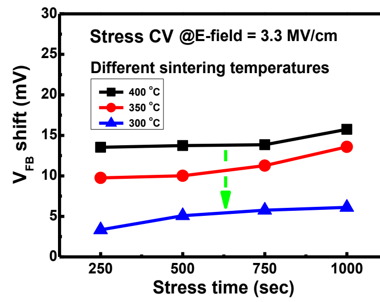

Fig. 11 Stress-induced V_{FB} shifts of Ge MOS devices with different sintering temperatures, showing the improved reliability of HfON gate dielectric.

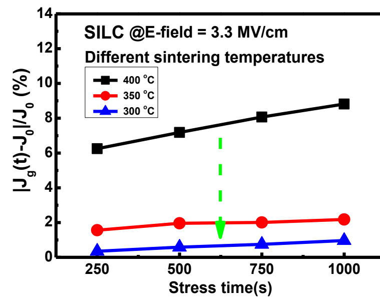

Fig. 12 Stress-induced leakage currents of Ge MOS devices with different sintering temperatures, indicating the improvement on the interface quality.