Analytical Capacitance Modeling and Simulation of Dual material- Graded channel -Gate stack Cylindrical/Surrounding (DMGCGS CGT/SGT) MOSFET

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Scaling of device dimensions into nano regime degrades the gate controllability over the drain current and increases short channel effects (SCEs). Various novel structures have been proposed to alleviate the aforementioned problem. Cylindrical/surrounding gate (CGT/SGT) MOSFET [1] is the one of the most attractive and deserving candidate for future Ultra Large Scale Integration (ULSI) applications due to its better SCEs immunity and gate controllability. The incorporation of dual material gate in CGT/SGT MOSFET overcomes the device degradation due to high electric field at the drain end. High metal work function on the source side (4.8 eV) and low work function on the drain side (4.4 eV) enhance the performance of the device and improves the carrier transport efficiency [2]. Although CGT/SGT MOSFET with dual gate material shows superior immunity against the SCEs, but still SCEs are not negligible for such device. Due to decreasing gate oxide thickness, the gate leakage problem increases. To reduce gate leakage current, high-k gate dielectric is mostly used as an alternative to replace SiO_2 as the gate dielectric. In gate stack architecture, material with high dielectric constant are introduce over the thin oxide layer to increase the effective thickness and decrease the physical thickness of the oxide layer thereby reducing gate leakage current. In Graded channel, high doping profile at the source side and low doping profile at the drain side, enhance the concentration of electron on the source side and increases the mobility of carrier on the drain side. A lot of research work related to analog/RF and capacitance has been done for CGT/SGT MOSFET but capacitance modeling for combined design Dual material-Graded channel-Gate stack Cylindrical/Surrounding (DMGCGS CGT/SGT) MOSFET has not been done yet. The capacitance model is essential to operationalise the device in the high frequency regime.

So in this paper, an analytical charge and capacitance model for DMGCGS CGT/SGT MOSFET has been presented. Impact of graded channel, gate stack with dual material has been analyzed using unified charge control based model derived from Poisson's equation. The charge partition on the source side and drain side in different regions of the device operation i.e. sub threshold region, linear region and saturation region are determined which follow the channel charge partition of Ward and Dutton [3]. The gate to source capacitance, C_{gs} and gate to drain capacitance, C_{gd} are calculated with respect to gate to source voltage by Atlas-3D simulator. It is analysed from the figures that the I_{on} and I_{off} current ratio increased in the above combination in comparison to bulk cylindrical MOSFET. The drain current, charges and capacitances are the function of applied voltages [4]. The model shows an improvement in drain current for DMGCGS CGAA MOSFET as compare to SMG MOSFET at various channel lengths. The results so obtained are in good agreement with the simulated data. Some important equations of the analytical modeling are giving below.

References

[1] A. Kranti, S. Haldar, R.S. Gupta., An accurate 2D analytical model for short channel thin film fully depleted cylindrical/surrounding gate (CGT/SGT) MOSFET, *Microelectronics Journal 32 (2001) 305–313.*
[2] P. Ghosh, S. Haldar, R.S Gupta, M. Gupta, "An analytical drain current model for dual material engineered cylindrical/surrounded gate MOSFET," *Microelectronics Journal 43 (2012) 17–24.*
[3] D. E. Ward and R. W. Dutton, " A Charge-Oriented Model for MOS Transistor Capacitance" IEEE *Journal of Solid State Circuits, VOL. sc-13, 1978.*
[4] O. Moldovan, B. Iniguez, D. Jimenez and J. Roig "Analytical charge and capacitance models of undoped cylindrical Surrounding – Gate MOSFETs" IEEE Transaction On Electronic Devices, Vol,54,No. 1, January 2007.

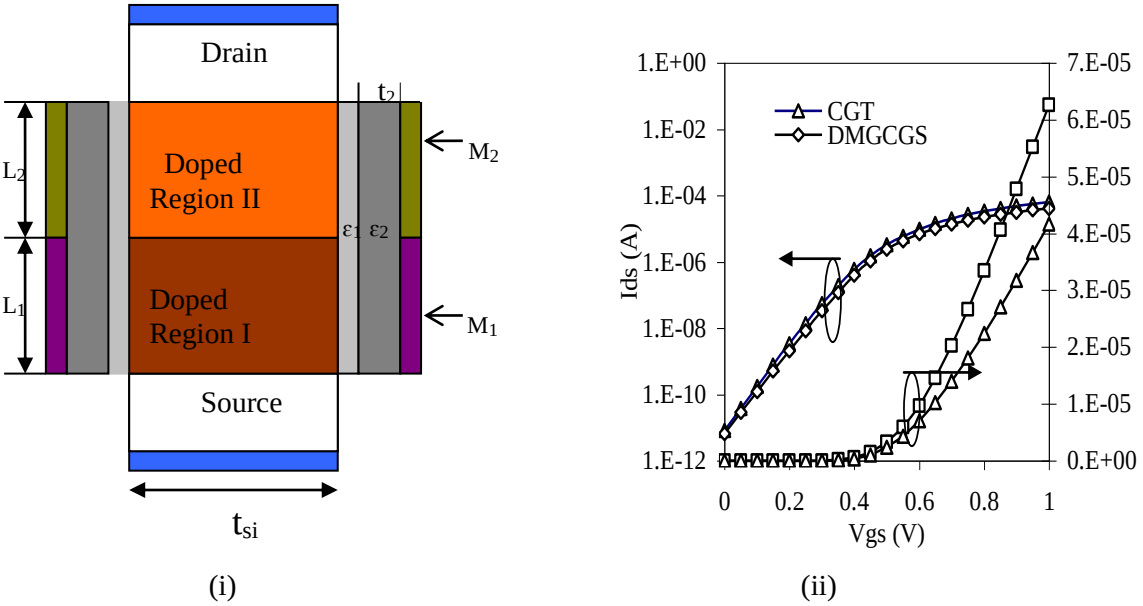

Fig 1(i) A Two dimensional structure of DMGCGS CGT/SGT MOSFET (ii) Drain current variation with respect to gate to source voltage. (R=10 nm, t_1=2 nm, t_2=2 nm, Na I=10^{17} cc^3 and Na II=10^{15} cc^3, L=30 nm, V_{ds}=0.5 V, concentration dependent mobility 1300 cm.

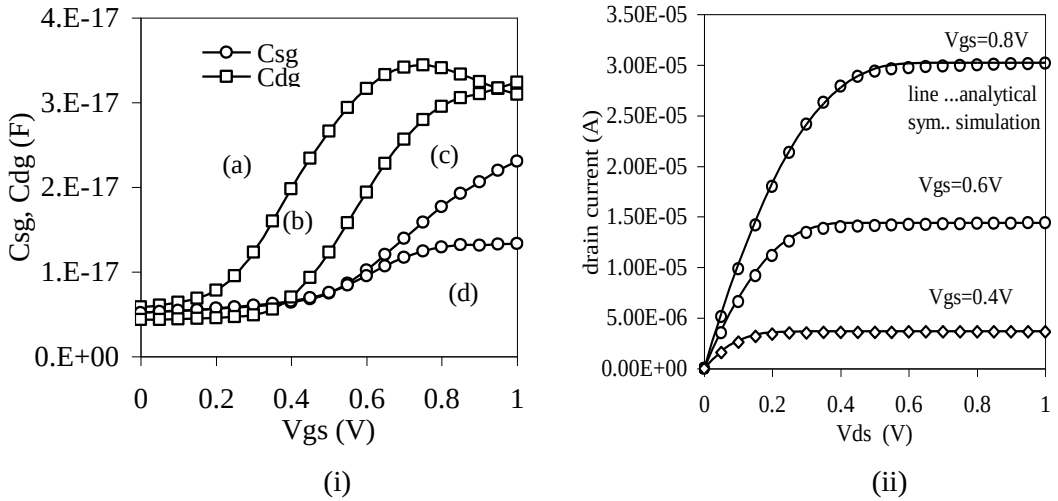

Fig 2(i) Variation of capacitances of with respect to gate to source voltage (a) and (c) drain to source capacitance and source to drain capacitance at V_{ds}=0.1 V (b) and (d). Drain to source capacitance and source to drain capacitance at V_{ds}=1V. (ii) Drain current with respect to drain to source voltage at different V_{gs} value.

Table (1) DM-GC-GS CGT MOSFET

V_{gs} = 1 V	**V_{ds} = 0.1mV V, Cut of region**	**V_{ds} = 0.4 V, Linear region**	**V_{ds} = 1 V, saturation region**
Q_{TG}	0.354	0.227	0.227
Q_s	0.177=50% of Q_{TG}	0.139=61% of Q_{TG}	0.139=61% of Q_{TG}
Q_d	0.177=50% of Q_{TG}	0.089=39% of Q_{TG}	0.088=39% of Q_{TG}

Table-1 shows the variation of charges in different region which follow the Ward-Dutton charge partition i.e. 3/5 on the source side and 2/5 on the drain side of the total charges when the transistor in on situation.