Student Paper

Degradation of 4H-SiC IGBT Threshold Characteristics Due to SiC/SiO_2 Interface Defects

Iliya Pesic[a], Dondee Navarro[b], Masataka Miyake[a], and Mitiko Miura-Mattausch[a]

[a] *Hiroshima University, 1-3-1 Kagamiyama, Higashi-Hiroshima 739-8530 Japan, iliya.pesic@gmail.com,*
[b] *SILVACO Japan, 4F Miyake Bldg. 549-2 Shinano-cho, Totsuka-ku, Yokohama 244-0801 Japan*

Abstract Reported measurements of the interface state density D_{it} at the 4H-SiC/SiO_2 interface and carrier recombination in the SiC substrate are incorporated in the simulation of a 4H-SiC IGBT trench device. Cross-sectional simulation results show two important degradation characteristics on the conduction current; reduction of magnitude due to the shallow traps and shift of threshold voltage towards higher gate voltages due to the deep traps. The wide bandgap of SiC and high interface defect density magnitude of available SiC/SiO_2 technology make SiC-based devices prone to degradation as compared to typical Si technology with a dominating homogeneous shallow-type trap.

Introduction Two types of defects are known to occur during fabrication of SiC-based devices; process-induced defects from the SiC/SiO_2 interface during trench formation, and structural defects which are related to crystallographic imperfections in the SiC substrate [1, 2]. The maximum D_{it} from a reported measurement occurred at the SiC/SiO_2 interface, reaching ~$10^{13}cm^{-2}eV^{-1}$[3]. Conventional Si/SiO_2 technology only has ~$10^{11}cm^{-2}eV^{-1}$. Such a high D_{it} for SiC creates a serious problem for device performance and therefore, needs to be investigated. In this work, we perform a simulation-based investigation of the threshold characteristics of the 4H-SiC IGBT trench device structure shown in Fig. 1. The reported measured 4H-SiC/SiO_2 defect density is included as interface defect states in the bandgap which are self-consistently solved in the Poisson equation [4]. The structural defects in the substrate are included using the Auger recombination model.

Simulation including Defects and Analysis

A. 4H-SiC/SiO_2 Interface Defects Measurements of D_{it} at the interface show four distinct peaks as illustrated in Fig. 2 [3]. In this report, we focus only on the acceptor-like traps D1 and D2 because they act on electrons, which are the carriers in the device considered. D1 is treated as a Gaussian distribution and D2 as an exponential tail distribution. As shown in Fig. 3, with defects, two phenomena can be observed in the threshold *IV* characteristics: the magnitude of the current is decreased, and the onset of conduction of current is shifted towards higher gate voltages V_g. These effects can be explained by the fact that the carriers responsible for inversion are impeded by being trapped in the defects. At low V_g, the deep trap D1 causes the conduction of current to shift towards higher gate voltages. At high V_g, the shallow trap D2 changes the current magnitude. These observations are explained in the band-diagram shown in Fig. 4. As V_g is increased, the quasi-Fermi level moves towards the conduction band thereby encountering the shallow traps. The separation of the deep and shallow trap effects can be observed in SiC because the defect densities are distinct and separated apart as can be seen in Fig. 2. To determine the region where the defects become most effective, three local interface areas in the device are defined as shown in Fig. 5. A1 at the edge of the oxide reduces the magnitude of the current as depicted by the arrows in Fig. 6. A2 at the oxide region above the channel shifts and changes the slope of the current. A3 has no significant impact. Most of the effect comes from the area under the channel where a high concentration of carriers is present.

B. Structural Defects in the 4H-SiC substrate Structural defects in the substrate introduce recombination sites for carriers. To consider this phenomenon, the Auger recombination model in the 4H-SiC material with recombination constants from [5] is included in the simulation. An insignificant reduction in the current is observed as shown in the inset figure in Fig. 7.

Discussion Process-induced interfacial defects lead to a significant degradation of the threshold *IV* characteristics of a 4H-SiC IGBT device. The wide bandgap of SiC makes the problem caused by defects serious because distinct shallow and deep traps are present aside from a high defect density magnitude. For Si, the defect density has a low magnitude and a rather homogeneous shallow-type trap only with no

distinct deep traps. As such, the only visible effect for Si is a reduction in the current magnitude as shown in Fig. 8, if the defect density magnitude is increased to a higher value.

For the SiC-IGBT device considered, the threshold voltage measured at collector current I_c = 1μA in Fig. 3, is shifted by 5V which is due to deep traps. Therefore, measurement of the deep trap density alone can be used to predict the amount of threshold voltage shift.

Summary We have investigated the effect of interfacial defects in 4H-SiC IGBT by including measured density of interface states in the device simulation. Process-induced defects occurring at the oxide interface are the most serious cause of threshold *IV* characteristics degradation.

References

[1] S. T. Pantelides, et al, "Si/SiO_2 and SiC/ SiO_2 Interfaces for MOSFETs – Challenges and Advances," *Materials Science Forum* 2006, Vols. 527 – 529, pp. 935 – 948.

[2] P. G. Neudeck, "Electrical Impact of SiC Structural Crystal Defects on High Electric Field Devices," *Materials Science Forum* 2000, Vols. 338 – 342, pp. 1161 – 1166.

[3] V. V. Afanasev, et al, "Intrinsic SiC/SiO_2 Interface States," *Physica Status Solidi (a)*, Vol. 162, pp. 321 – 337, July 1997.

[4] *VICTORY User's Manual*, SILVACO, Inc., Santa Clara, CA, 2013.

[5] A. Galeskas, et al, "Evaluation of Auger Recombination Rate in 4H-SiC," in *Proc. Intl. Conf. on SiC, III-Nitrides and Related Materials*, 1997, pp. 533-536.

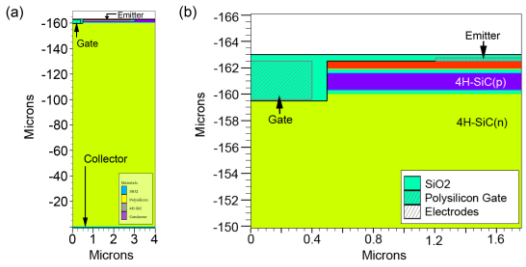

Fig. 1. 4H-SiC IGBT trench device structure. (a) cross-section, and (b) enlarged image of the channel region.

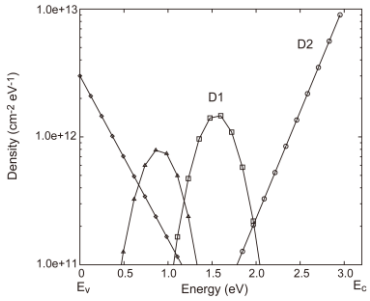

Fig. 2. Measured density of interface states at 4H-SiC/SiO_2 interface. Only acceptor-like traps D1 and D2 are considered because electrons are the carriers in the device simulated.

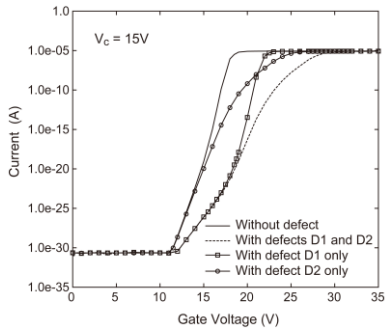

Fig. 3. Effect of each density on the threshold *IV* characteristics.

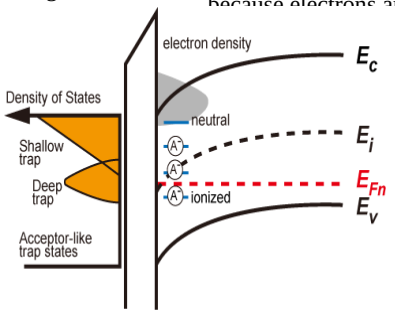

Fig. 4. Band diagram showing the trapping mechanism towards shallow traps. At high V_g, the band bending becomes pronounced and the E_{Fn} moves toward conduction edge and thereby carriers encounter shallow traps.

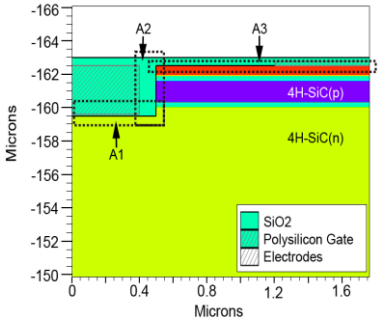

Fig. 5. Specified local SiC/SiO_2 interface areas where the defect densities are activated.

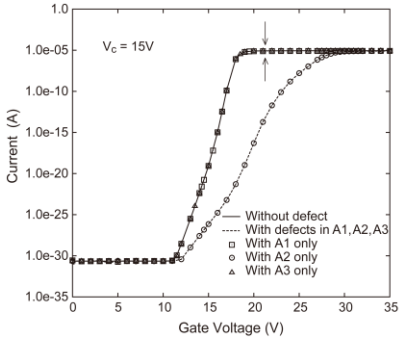

Fig. 6. Dependence of the threshold characteristics on the local SiC/SiO_2 interface areas. A2 shifts and changes the slope of the current.

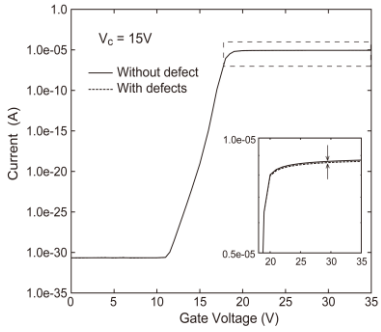

Fig. 7. *IV* characteristics simulated with and without defect in the SiC substrate. Insignificant decrease in magnitude of the current is observed.

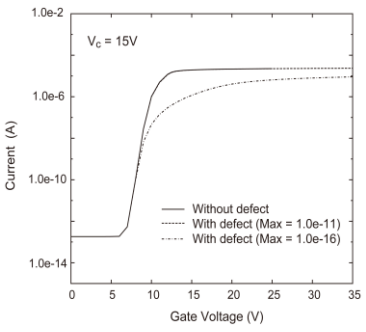

Fig. 8. Effect of defect states in Si device. Only dominating shallow trap is considered in the simulation.