Electron mobility improvement due to GaO_x passivation layer formed by pre-deposition annealing in $HfO_2/In_{0.53}Ga_{0.47}As$ nMISFET with sub-1.0 nm EOT

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The electron mobility of HfO_2/InGaAs nMSIFETs has been found to be significantly enhanced by pre-deposition annealing before atomic layer deposition (ALD) of HfO_2 and the record high electron mobility in sub-1.0 nm EOT regime has been demonstrated. XPS measurements revealed that the pre-deposition annealing increased GaO_x and reduced AsO_x at the MIS interface, which was considered to result in the reduction of D_{it} as well as charge traps.

InGaAs nMISFETs are attracting much attention for the alternative to Si nMISFETs because of their high electron mobility. Although HfO_2 (k ~ 20) is suitable for EOT scaling [1, 2], it has been reported that the mobility of InGaAs surface channel MISFETs with HfO_2 gate dielectric is much lower than that with Al_2O_3 (k ~ 9). The lower mobility is due to interface states and/or roughness [3-5]. In this study, we propose a simple way, pre-deposition annealing before HfO_2 deposition, to effectively improve HfO_2/InGaAs MIS interface quality and increase the mobility.

Fig. 1 shows a schematic of $HfO_2/In_{0.53}Ga_{0.47}As$ nMISFET and its cross sectional TEM image. The device was fabricated as follows. An $In_{0.53}Ga_{0.47}As$ substrate with $N_a = 3x10^{16}$ cm^{-3} was pretreated with $(NH_4)_2S$ for 2 min and successively loaded into an ALD chamber. The substrate was annealed at 300 ^oC for 30 min in Ar atmosphere (5 torr) just after loading. Then it was cooled down to 200 ^oC and 50-cycle HfO_2 (~4.0 nm) was deposited. In a reference sample, 50-cycle HfO_2 was deposited at 200 ^oC just after loading.

A gate metal, TaN 20 nm, was deposited after HfO_2 deposition. Gate was defined by RIE and self-aligned Ni-InGaAs alloyed S/D contacts were formed by N_2 annealing at 350 ^oC for 5 min. Al SD contact and back contact was formed for a reduction of contact resistance.

Surface chemical states of HfO_2/InGaAs investigated by XPS measurements are shown in Fig. 2(a). It is clearly seen that an intensity of GaO_x peak is increased by the pre-disposition annealing, indicating the formation of interfacial GaO_x layers during annealing. The thickness of GaO_x estimated by XPS [6, 7] was <0.23 nm with the annealing. On the other hand, an AsO_x peak shows slight reduction with the annealing. These phenomena could result from the oxidation of Ga atoms by residual oxidant (H_2O) and the thermal desorption of unstable AsO_x (Fig. 2(b)).

Fig. 3 shows gate to channel capacitance, C_{gc}, characteristics measured from 1 kHz to 100 kHz. It is seen that the annealed sample has much smaller frequency dispersion around flat band voltage, suggesting the reduction of D_{it} in band gap [5, 8]. Besides, the annealed sample has much smaller hysteresis than that in the un-annealed sample (Fig. 4), indicating that the pre-deposition annealing decreases not only D_{it} but also the charge trap density. These results are attributable to the effective passivation by the thin interfacial GaO_x layer, as suggested by Jevasuwan et al. [7]. No C_{gc} reduction due to the pre-deposition annealing suggests no EOT penalty caused by the thin interfacial GaO_x layer formed here. In fact, the EOT of pre-deposition annealed one was estimated to be 0.6 nm by fitting its $C_{gc-100kHz}$. Gate leakage was also confirmed to be almost unchanged by the pre-deposition annealing and it is four orders of magnitude smaller than that of Al_2O_3/InGaAs in sub-1.0 nm regime (Fig. 5). Fig. 6 shows I_d-V_d characteristics of both devices with and without the pre-deposition annealing. Substantial increase of I_d by pre-deposition annealing is observed. Inversion-layer electron mobility against surface carrier density, N_s, is shown in Fig. 8. The mobility is confirmed to be significantly enhanced by the pre-deposition annealing (Fig. 7), which is thanks to the improved MIS interface quality as seen in Figs 3 and 4. Fig. 8 summarizes EOT-mobility trend of $In_{0.53}Ga_{0.47}As$ nMISFETs with Al_2O_3 and HfO_2 gate dielectrics, including the values reported by the other groups. Our device with HfO_2 shows the highest mobility in the sub-1 nm EOT regime. It is, therefore, concluded that HfO_2/InGaAs nMIFETs with pre-deposition annealing is promising to realize high mobility InGaAs nMISFETs with extremely thin EOT.

Acknowledgements
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References

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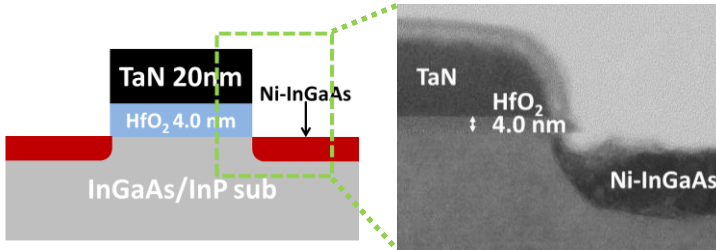

Fig. 1 A schematic of HfO_2/InGaAs nMISFET and its cross sectional TEM image.

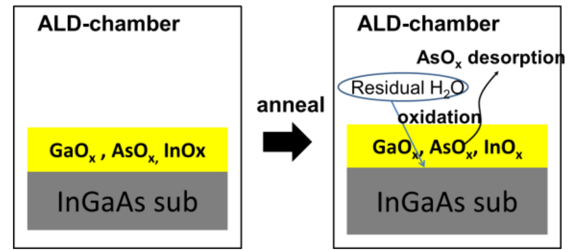

Fig. 2(b) A model of the GaO_x formation and AsO_x desorption in an ALD chamber.

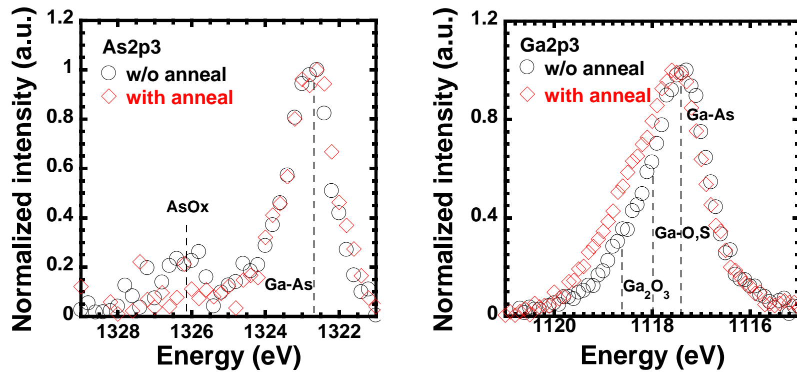

Fig. 2(a) As2p3 (left) and Ga2p3 (right) peak measured by XPS for HfO_2 10cycle/InGaAs with and without pre-deposition annealing.

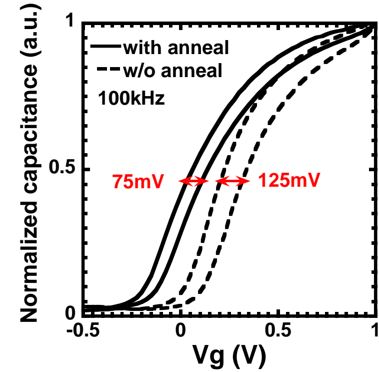

Fig. 4 Hysteresis of C_{gc} for each device measured at 100 kHz.

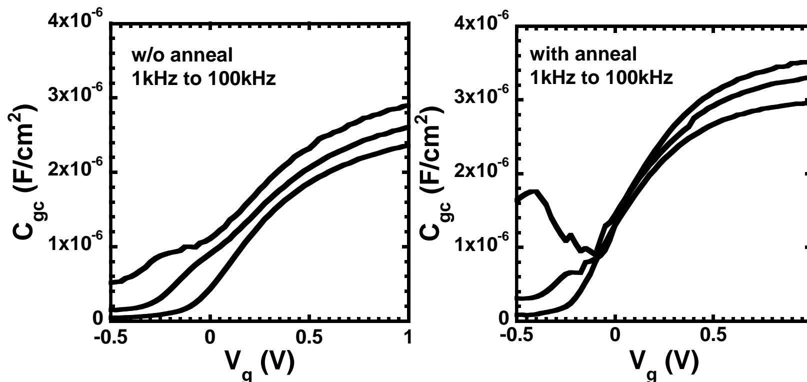

Fig. 3 C_{gc}-V_g plot of HfO_2/InGaAs nMSIFET with and without pre-deposition annealing.

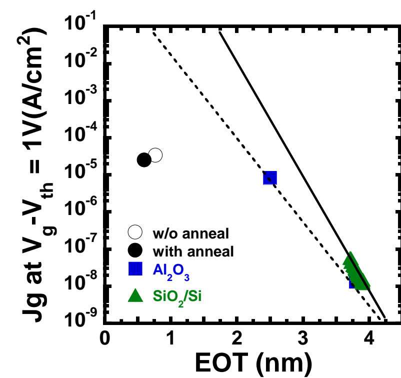

Fig. 5 J_g at V_g-V_{th} = 1V in HfO_2, Al_2O_3/InGaAs and SiO_2/Si nMOSFET.

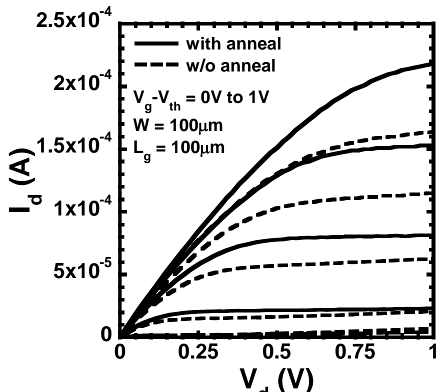

Fig. 6 I_d-V_d characteristics of devices with and without pre-deposition annealing.

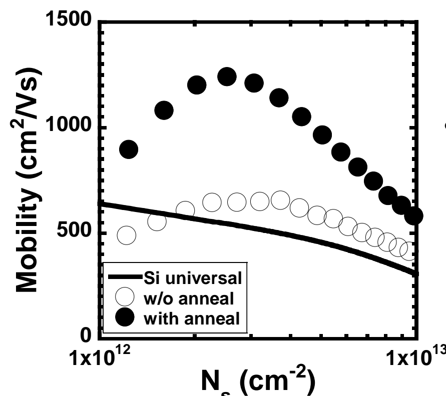

Fig. 7 Electron mobility against surface carrier density, N_s, of devices with and without pre-deposition annealing.

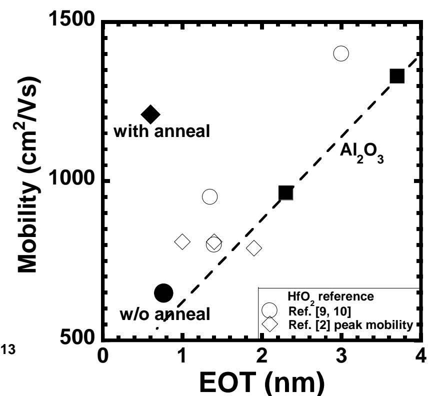

Fig. 8 Mobility v.s EOT for various gate-stack at $N_s = 3x10^{12}$ cm^{-2}. Black solid dots represent data of this work.