Student Paper

Source-drain distance scaling and its effect on fringing capacitance in ultra-high speed GaN HEMTs

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GaN-based high-electron-mobility transistor (HEMT) cutoff frequencies have been boosted over 400 GHz by aggressively scaling the gate length, L_g, to below 30 nm [1,2] and the source-drain distance, L_{sd}, to ~ 100 nm [2]. However, for gate lengths below 100 nm, the parasitic charging delay caused by source and drain access resistances and gate fringing capacitance can account for a large fraction of the total delay [3]. The access resistance issue has been addressed by employing barriers such as InAlN and InAlGaN [4] and regrown n^+ GaN contacts [5]. In this paper, the impact of source-drain distance scaling, its effect on gate fringing capacitance, and the resulting impact on the high frequency performance of T-gate recessed InAlN HEMTs is investigated. We observe that scaling the source-drain distance reduces the parasitic resistance, but also increases the fringing capacitance. Consequently, the speed of devices with unscaled L_{sd} and that of devices with scaled L_{sd} become comparable in the limit of short gate length scaling due to this tradeoff in fringing capacitance.

For the devices reported here, graded n^+ InGaN/GaN regrown ohmic contacts were used; E-mode operation is achieved by gate recessing. The details of the process flow have been described in [6,7]. The un-scaled/scaled devices have L_{sd}'s of ~0.72/0.13 μm and L_g's of ~40/24 nm as shown in Fig.1 (a) and (b), respectively. A dielectric etch-back process was applied for the scaled devices to completely remove the dielectric under the T-gate cap to minimize parasitic capacitances.

The DC and small signal RF characteristics for a scaled-L_{sd} device are shown in Fig. 2; characteristics of an un-scaled device in an otherwise identical process flow have been reported in [7]. From delay time analysis [3], it was found that the parasitic delay for the un-scaled/scaled device is 0.39/0.28 ps. This parasitic delay represents more than 50% of the total delay time for both devices. Equivalent circuit parameters (ECPs) extracted from on-wafer s-parameter measurements are shown in Table 1; from these ECPs and the equation [3]

$$\tau_{par}=(C_{gs,ext}+C_{gd,ext})/g_m+C_{gd}\,(R_s+R_d)+(C_{gs}+C_{gd})(R_s+R_d)g_{ds}/g_m\,, \quad (1)$$

one can see that the dominant parasitic delay time originates from the extrinsic fringing capacitances $C_{gs,ext}$ and $C_{gd,ext}$. Simulation of $C_{gs,ext}$ and $C_{gd,ext}$ was performed in COMSOL based on the gate geometry extracted from TEM and a 2DEG depletion estimated from TCAD simulations for both devices. $C_{gs,ext}/C_{gd,ext}$ were estimated to be ~ 260/162 fF/mm for the unscaled device, consistent with the extracted values of 238/161 fF/mm from measured *S*-parameters under coldFET bias conditions. Assuming that $C_{gs,ext}$ and $C_{gd,ext}$ are independent of bias, the intrinsic capacitances are then estimated by subtracting the extracted $C_{gs,ext}/C_{gd,ext}$ from the total C_{gs} and C_{gd} ECPs. From this analysis, we find that $C_{gs,ext}/C_{gd,ext}$ account for ~40% of the total gate capacitance. Moreover, the COMSOL simulation results also suggest that $C_{gs,ext}$ / $C_{gd,ext}$ can be lowered to ~ 160/101 fF/mm when the gate stem height is increased to ~200 nm and the dielectric surrounding the gate is removed (the SiON relative permittivity ε_r is assumed to be 5). On the other hand, for the scaled-L_{sd} device the extrinsic parasitic capacitances are higher due to the close spacing between the contacts (see Fig.1); even with a gate stem ~170 nm tall and no dielectric under the gate, the fringing capacitance extracted from *S*-parameters is about 194/158 fF/mm, higher than 160/101 fF/mm in the unscaled L_{sd} device. Based on this understanding, we estimate the speed of an unscaled-L_{sd} device but with the gate length decreased from 40 nm to 24 nm and optimized fringing capacitances of 160/101 fF/mm. An f_T of 340 GHz is expected, which is comparable to that of the scaled-L_{sd} device, ~ 339 GHz. This analysis provides new insight about the source drain distance scaling and highlights the significance of fringing capacitance in ultra-high speed HEMTs. It also suggests that maximizing intrinsic g_m is the key to further minimizing the dominant $(C_{gs,ext}+ C_{gd,ext})/g_m$ term in Eqn.(1).

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References

[1] Y. Yue, et. al., " Ultrascaled InAlN/GaN High Electron Mobility Transistors with Cutoff Frequency of 400 GHz," *Jpn. J. Appl. Phys*, vol. 52, no. 8, pp. 08JN14-1 - 08JN14-2, Aug. 2012

[2] K. Shinohara, et. al., "Self-Aligned-Gate GaN-HEMTs with Heavily-Doped n+-GaN Ohmic Contacts to 2DEG", in *Proc. IEEE IEDM*. 27.2.1-27.2.4, 2012.
[3] B. Sensale-Rodriguez, et.al., "Time delay analysis in high speed gate-recessed E-mode InAlN HEMTs," *Solid-State Electronics*, vol. 80, pp. 67-71, 2013
[4] R. Wang, et. al., "220-GHz quaternary barrier InAlGaN/AlN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1215-1217, Sept. 2011
[5] J. Guo, et. al., "MBE regrown ohmics in InAlN HEMTs with a regrowth interface resistance of 0.05ohm-mm," *IEEE Electron Device Lett.*, vol. 33, no. 4, pp. 525-527, April 2012.
[6] M. Schuette, et. al., "Gate-Recessed Integrated E/D GaN HEMT Technology With f_t/f_{max} >300 GHz," *IEEE Electron Device Lett.*, vol.34, no.6, pp.741-743, June 2013
[7] B. Song, et. al., "Monolithically integrated E/D-mode InAlN HEMTs with f_t/f_{max} > 200/220 GHz," in *IEEE DRC Dig*., 2012

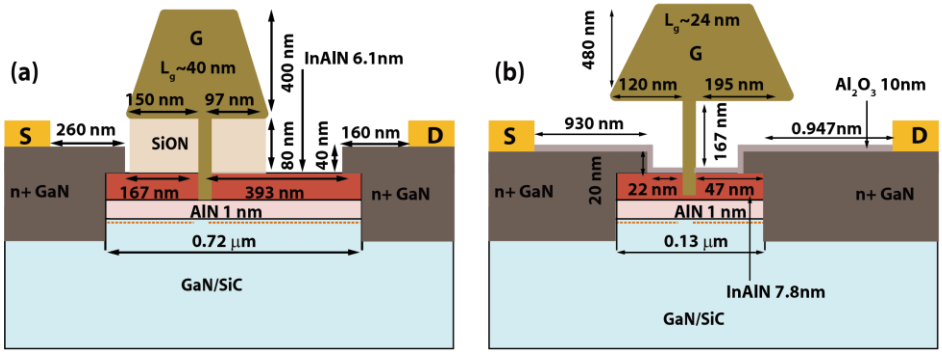

Fig.1 Schematic of the gate recessed E-mode InAlN HEMTs (not to scale): (a) unscaled L_{sd} (~0.72 μm) with L_g ~ 40 nm, (b) scaled L_{sd} (~0.13 μm) with L_g ~24 nm

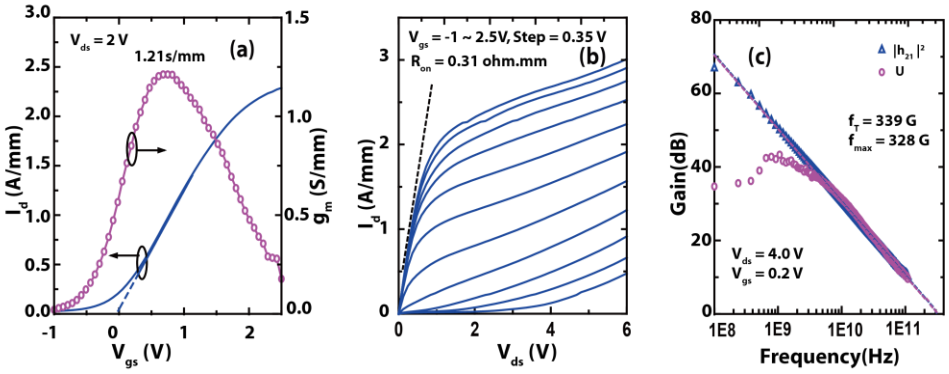

Fig.2 Scaled device characteristics: (a) transfer characteristics, (b) common source I-Vs, and (c) on-wafer small signal performance.

	40-nm un-scaled [7]	24-nm scaled	24-nm un-scaled projected
g_m (mS/mm)	1680	1638	1638
g_{ds} (mS/mm)	169	276	276
C_{gs} (fF/mm)	811	494	490
C_{gd} (fF/mm)	178	160	111
R_s (Ω.mm)	0.23	0.10	0.23
R_d (Ω.mm)	0.26	0.20	0.26
f_T (GHz) ECP	220	332	340
f_{max} (GHz) ECP	245	326	-
f_T (GHz) meas.	225	339	-
f_{max} (GHz) meas.	250	328	-

Table.1 Extracted equivalent circuit parameters of devices with unscaled and scaled source-drain distances.