Student Paper

An Analytical Core Model for Tapered Tri-Gate Fin Field-Effect Transistors

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Recently, the Fin field-effect transistors (FinFETs) have been extensively investigated because of their excellent electrical performance [1]. Many analytical models have been proposed to describe the current-voltage characteristics of the rectangular tri-gate FinFETs. However, due to the limitation of the lithography and etching techniques, the channel of the manufactured FinFETs always have a taper-shaped instead of a rectangular-shaped as shown in Fig. 1 [2]. In this work, an analytical core model of the tapered tri-gate FinFETs is developed and its accuracy is verified by the numerical simulation using a 3D Sentaurus Device simulator.

An analytical core model has been proposed for the regular rectangular tri-gate FinFETs by assuming an arbitrary channel potential profile [3]. In this model, the charges (mobile charge density Q_e and depletion charge density Q_d) in the channel and the device structure parameters (gate capacitance C_g, channel capacitance C_{ch} and area of channel A_{ch}) approximately satisfy the Eq. (1). Respect to the rectangular FinFETs, the tapered tri-gate FinFETs has a wider fin bottom width (W_B) respect to the fin top (W_T). The C_g, C_{ch}, A_{ch} and Q_d of the tapered tri-gate FinFETs are not only a function of the fin width and fin height (H), but also of the angle (θ) between the fin side and fin bottom. For the tapered tri-gate FinFETs, the C_g is estimated by the capacitance of a metal-insulator-metal (MIM) capacitor, which is obtained by replacing the channel with metal. The MIM is been divided into two parts combined in parallel: the top gate capacitor and the side gate capacitor. The top gate capacitor is treated as one-third of the square tri-gate capacitor with side-length W_T. The side gate capacitor is estimated by half of the square gate-all-around capacitor with side-length $H/\sin\theta$. So, utilizing the work of Ruiz [4], the C_{MIM} can be described by Eq. (2). A fitting parameter γ is included to optimize the model. As it is shown in Fig. 2 and Fig. 3 for a fixed γ=0.63, C_{MIM} shows good accuracy compared with the simulation results in a wide range of W_B, H, T_{ox} and θ. The C_{ch} is given by Eq. (4), in which the first and second terms are contributed by the two side gates and the top gate, respectively. A_{ch} and Q_d are described by Eqs. (5) and (6), respectively.

The Q_e can be solved from Eq. (1) for a certain bias condition. Then, the drain current of the tapered FinFET is obtained by analytically integrating Q_e from source to drain, as shown in Eq. (8) [5]. It has been found that the C_g can effectively affect the accuracy of the model and its value is under-estimated by C_{MIM}. In fact, the C_g is far more complex than C_{MIM}. The control capability of the gate to the channel is enhanced by the geometry effects, such as the corner effects. So, it's obvious that the desired C_g should be bigger than C_{MIM}. Therefore, to ensure the accuracy of the model, parameter β is introduced to take the gate enhancement into account as indicated in Eq. (3). α_n is another fitting parameter used to optimize the model [3]. By optimization, the α_n and β is been fixed at 2.3 and 1.1, respectively. As shown in Fig. 4 and Fig. 5, the model shows good accuracy with the numerical simulation at a wide range of structures (different W_B, H, θ) and bias conditions (V_{DS},V_{GS}).

In conclusion, an analytical core model of tapered tri-gate FinFETs is proposed. This model has an explicit and continuous expression in all the operation regimes. It shows good agreement with the numerical simulation for a wide range of device parameters and bias conditions.

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References

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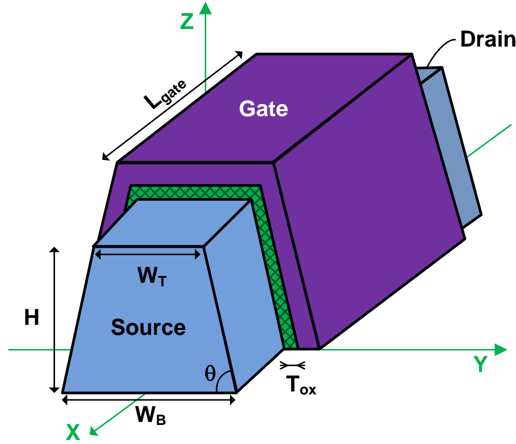

Fig. 1Schematic diagram of the tapered tri-gate field effect transistor.

Table. 1 The equations of the proposed model

$$V_{GS}-V_{FB}+\frac{Q_d}{C_g}-V=-\frac{Q_e}{C_g}+\upsilon_T\ln\left[\frac{Q_e\left(Q_e/\alpha_n+Q_d\right)/\upsilon_T C_{ch}}{qA_{ch}\frac{n_i^2}{N_{ch}}\left(1-\exp\frac{Q_e/\alpha_n+Q_d}{\upsilon_T C_{ch}}\right)}\right] \quad (1)$$

$$C_{MIM}=\frac{5\gamma\varepsilon_{ox}/2}{\ln\left(1+5\gamma t_{ox}\sin\theta/4H\right)}+\frac{3\gamma\varepsilon_{ox}/2}{\ln\left[1+3\gamma t_{ox}/\left(W_B-2H/\tan\theta\right)\right]} \quad (2)$$

$$C_g=\beta C_{MIM} \quad (3)$$

$$C_{ch}=2\tan\theta\varepsilon_{si}\ln\left(1-\frac{2}{\tan\theta}\right)+\varepsilon_{si}\left(\frac{W_B}{H}-\frac{2}{\tan\theta}\right) \quad (4)$$

$$A_{ch}=HW_B-H^2/\tan\theta \quad (5)$$

$$Q_d=-qN_{ch}A_{ch} \quad (6)$$

$$I_{DS}=-\frac{\mu}{L_{gate}}\int_{Q_{e,S}}^{Q_{e,D}}Q_e\frac{dV}{dQ_e}dQ_e \quad (7)$$

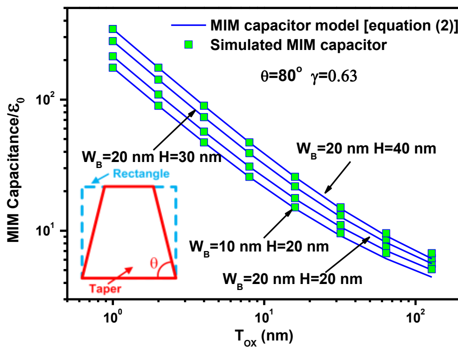

Fig. 2 Simulated capacitance of the tapered tri-gate MIM capacitor (symbol) as the function of the oxide thickness. Its comparison with the analytical model is also included (line). Inset: structure of the rectangular tri-gate (blue) used as a comparison of tapered tri-gate (red) and the definition of θ.

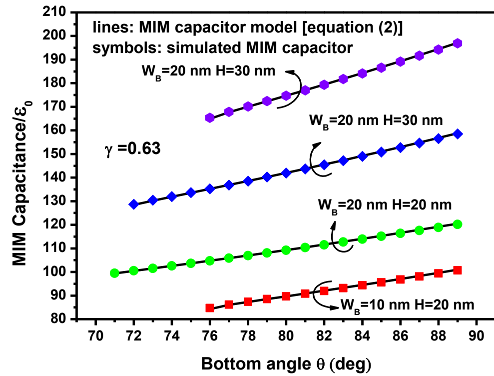

Fig. 3 The capacitance of the tapered tri-gate MIM capacitor versus θ obtained from the analytical model (line) and the numerical simulation (symbol). Curves of different fin size are included.

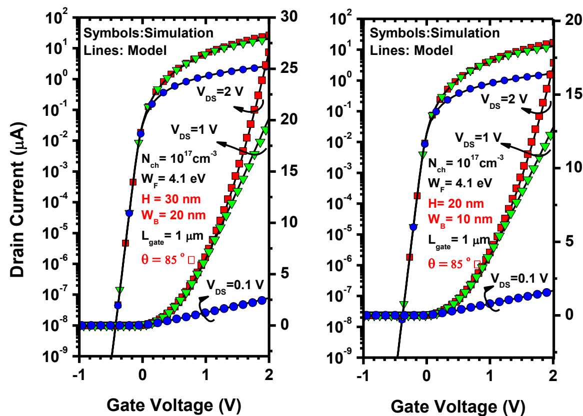

Fig. 4 The transfer characteristics of the tapered FinFET obtained from the proposed model and the numerical simulation. The θ is the same but the size of the silicon fin is different for the left and right figure.

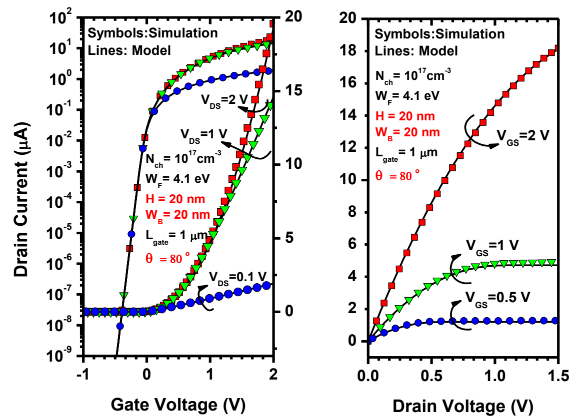

Fig. 5 The transfer characteristic (left) and output characteristic (right) of the tapered FinFET. The fin size is 20×20 (W_B×H, nm) and θ=80 °.