Student Paper

Double-gate Tri-layer PEALD ZnO TFTs

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We previously reported double-gate ZnO thin film transistors (TFTs) with plasma enhanced atomic layer deposition (PEALD) Al_2O_3 as bottom dielectric, PEALD ZnO as active layer, and ALD Al_2O_3 as top dielectric [1]. ALD Al_2O_3 was used for the top gate dielectric instead of PEALD Al_2O_3 because end-of-process Al_2O_3 passivation causes turn-on voltage and threshold voltage shifts and ALD Al_2O_3 causes a much smaller shift than PEALD Al_2O_3 [2-3]. We have also reported tri-layer ZnO TFTs with PEALD Al_2O_3 bottom dielectric, PEALD ZnO, and PEALD Al_2O_3 passivation layer deposited in one deposition run without breaking the vacuum that have small turn-on and threshold voltage shifts compared to unpassivated devices [4]. In this paper we extend the tri-layer process and report double-gate, tri-layer PEALD ZnO TFTs.

The double-gate, tri-layer PEALD ZnO TFTs were fabricated on borosilicate glass substrates. Chromium gate electrodes were deposited by ion beam sputtering and patterned by wet etching. Next, PEALD at 200 °C was used to deposit a 32 nm-thick Al_2O_3 bottom gate dielectric layer, a 10 nm-thick ZnO active layer, and a 32 nm-thick Al_2O_3 top gate dielectric layer. All three layers were deposited in one run without breaking vacuum. Next, windows for contacts and vias in the top Al_2O_3 passivation layer were patterned by photolithography. The Al_2O_3 needs to be selectively etched without damaging the ZnO active layer. An aqueous alkaline solution with pH between 10 and 12, with Al_2O_3 etch rate of 10 - 20 nm/min at 55 °C and near zero etch rate for ZnO was used for this step. Next, titanium source/drain electrodes were deposited by sputtering and patterned by lift-off, and the ZnO active layer was patterned by photolithography and wet etching. Finally, titanium top gate electrodes were deposited by sputtering and patterned by lift-off. A schematic cross-section and microscope image of a finished device are shown in Figure 1.

Because the top gate for the double-gate, tri-layer PEALD ZnO TFT does not overlap the device source and drain contacts, it is necessary to use the bottom gate to accumulate carriers to allow large device currents. With the top and bottom gates connected together, the maximum linear region mobility is >30 $cm^2/V{\cdot}s$ and the turn-on voltage is near 0 V (Figure 2, left). With the top gate held at 0 V and the bottom gate swept, the maximum linear region mobility is about 20 $cm^2/V{\cdot}s$ and the turn-on voltage is about -1.5 V. The top gate voltage can be used to tune the turn-on and threshold voltage for the double gate device. As Figure 3 (left) shows, for negative top gate bias, threshold voltage and turn-on voltage are effectively tuned. This is because with the top gate biased negative the top gate region of the device turns on last with increasing bottom gate voltage. As the top gate bias is varied from 0 V to -4 V the turn-on voltage is tuned from about -1.5 V to about 1 V. Positive top gate bias (Figure 3, right) does not tune the TFT turn-on voltage. This is because with the top gate biased positive the device turn-on is controlled by the region of the channel not gated by the top gate. However, increasing the top gate bias will decrease the resistance of the top-gate-region of the TFT channel and increase the device current (Figure 3, right).

The double-gate, tri-layer PEALD ZnO TFT structure reported here allows tuning of the TFT turn-on and threshold voltage. This can be used, for example, to allow enhancement/depletion mode circuits simply by controlling the local top gate voltage. These devices also provide improved off-state electric field confinement which can improve device stability. The tri-layer process allows high-quality PEALD Al_2O_3 to be used for both top and bottom gate dielectrics and produces TFTs with reduced turn-on and threshold voltage shift compared to end-of-process passivated devices.

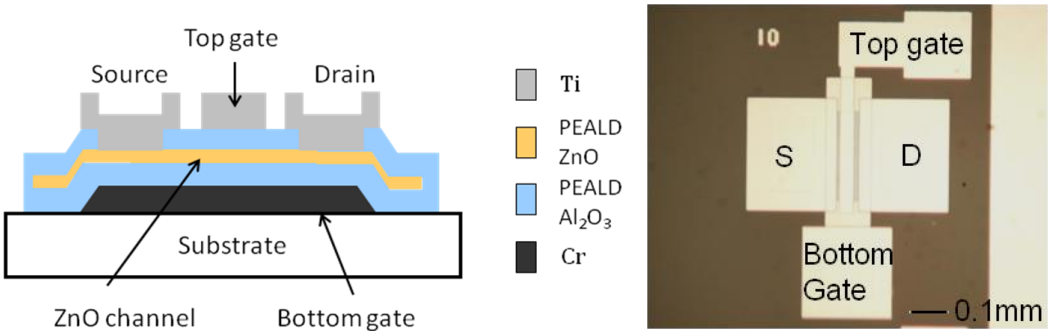

Fig. 1 (left) PEALD double-gate tri-layer TFT cross-section, (right) microscope image of PEALD double-gate tri-layer TFT.

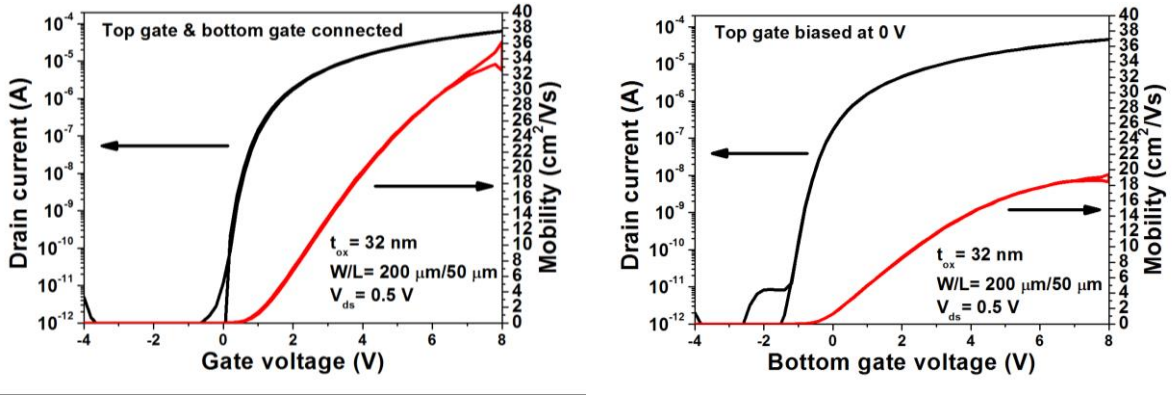

Fig. 2 Linear region drain current (log scale) and field-effect mobility (linear scale) versus gate voltage of PEALD double-gate tri-layer TFT with (left) top and bottom gates connected together and (right) bottom gate swept with top gate held at 0 V.

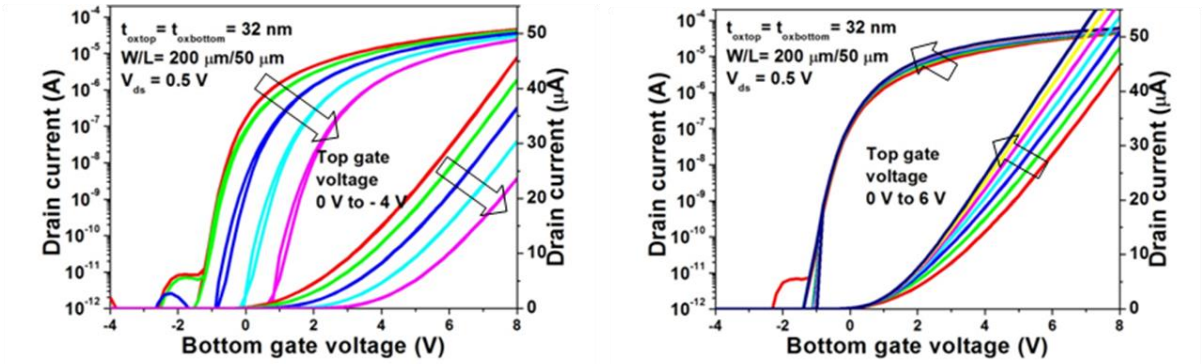

Fig. 3 Drain current versus bottom gate voltage of PEALD double-gate tri-layer TFT with top gate voltages of (left) 0 V to -4 V and (right) 0 V to 6 V.

References

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