**Student Paper**

# Two-Bit SRAM Cell Based on the Multi-State Quantum Dot Gate SOI FETs

M. Lingalugari[a], P-Y. Chan[a], J. Chandy[a], E. Heller[b], and F. Jain[a]

[a] *Electrical and computer Engineering, University of Connecticut, Storrs, CT, USA, murali.lingalugari@uconn.edu*
[b] *Synopsys Inc., Ossining, NY, USA.*

The latest microprocessor architectures incorporate very large on-chip cache memories to reduce the off-chip memory accesses which improve the performance and the speed of the microprocessors [1]. The majority of the cache memories comprise of the SRAM cells. The reduction in SRAM cell area provides the space to accommodate more number of cells leading to the increment in the cache memory without increasing the die size. The SRAM cell area can be reduced by utilizing multi-state transistors. Multi-state characteristics has been demonstrated by quantum well as well as quantum dot FETs like spatial wavefunction-switched FETs (SWSFETs), quantum dot gate FETs (QDGFETs) and quantum dot channel FETs (QDCFETs) etc [2-4]. In this paper we present the experimental results and the modeling of the 2-bit SRAM cell using 4-state QDGFET inverters.

The cross-sectional schematic of a 4-state QDGFET on silicon-on-insulator (SOI) substrate is presented in Fig. 1(a). 3-state characteristics has been demonstrated by using either $SiO_x$-cladded Si or $GeO_x$-cladded Ge dots on Si and InGaAs substrates [5-7] where as the 4-state behavior utilizing both Si and Ge (mixed-dot) QDs on Si substrate has been reported recently [8].The experimental $I_D$-$V_G$ and $I_D$-$V_D$ characteristics of a QDGFET are shown in Figs. 1(b) and 1(c) respectively [8]. In QDGFETs, the intermediate low current saturation states are available in addition to the conventional ON and OFF states. These intermediate states occurs when the charge carriers tunnel from the inversion channel to the quantum dots (QDs) present in the gate region through the thin gate insulator when the proper gate voltages ($V_G$) are applied. The charge present in the QDs will change the threshold voltage of the device, with the changing $V_G$ leading to the current saturation.

The number of the intermediate states can exhibit by the QDGFET is dependent on the material composition of the quantum dots (QDs). The voltage at which the intermediate states occur can be tuned by varying the size of the QDs, the cladding layers thicknesses and the gate insulator layer thickness and its material. The gate insulator can be the conventional $SiO_2$ or the high-κ (II-VI) dielectric layers [2-8]. The feasibility of fabricating the QDGFETs on SOI substrates are analyzed due to its lower source and drain to substrate capacitances, lower leakage, low power consumption and higher switching speeds compared to the bulk Si substrates [9]. Figure 2 shows atomic force microscope (AFM) image of the site-specifically self assembled (SSA) [10] QDs on the p-type patterned SOI substrate [11].

4-state QDGFET has two intermediate ($i_1$ and $i_2$), ON and OFF states, which is a quaternary output device. These intermediate states can be used as the logic states and the quaternary outputs can be easily translated to the binary states by employing the simple analog multiplexer circuits [12]. The schematic diagram of a QDGFET based SRAM cell employed using the conventional six transistors (6T) architecture shown in Fig. 3. Here the driver transistors are replaced by the QDGFET which will provide the quaternary outputs for the applied DC input voltage. These quaternary outputs are equivalent to four digital states or 2-bit binary output. By employing the conventional 6T architecture with QDGFETs 50% reduction in the cell area can be achieved as shown in the below table.

| Type of the transistors used in 2-bit SRAM cells | Number of Transistors in a 2-bit SRAM cell |
|---|---|
| 6T architecture with conventional FETs | 12 (8 FETs and 4 access transistors) |
| 6T architecture with QDGFETs | 6 (3 QDGFETs, 3 FETs) |

## References

[1] S. Rusu, S. Tam, H. Muljono, D. Ayers, J. Chang, R. Varada, M. Ratta, and S. Vora, "A 45nm 8-core enterprise Xeon® processor", *A-SSCC*, pp. 9–12, 2009.

[2] F.C. Jain, E. Suarez, M. Gogna, F. Al-Amoody, D. Butkiewicus, R. Hohner, T. Liaskas, S. Karmakar, P.-Y. Chan, B. Miller, J. Chandy, and E. Heller, "Novel Quantum Dot Gate FETs and Nonvolatile Memories Using Lattice-Matched II–VI Gate Insulators", *J. Electron. Mater.*, 38, 8, pp. 1574-1578, 2009.

[3] F. Jain, S. Karmakar, P-Y. Chan, E. Suarez, M. Gogna, J. Chandy, and E. Heller, "Quantum Dot Channel (QDC) Field-Effect Transistors (FETs) Using II-VI Barrier Layers", *J. Electron. Mater.*, 41,10, pp. 2775-2784, 2012.

[4] F.C. Jain, J. Chandy, B. Miller, E-S. Hasaneen, and E. Heller, "Spatial Wavefunction-Switched (SWS)-FET: A novel device to process multiple bits simultaneously with sub-picosecond delays", *Int. J. High Speed Electronics and Systems*, 20, 3, pp. 641-652, 2011.

[5] S. Karmakar, E. Suarez, and F. C. Jain, "Three-State Quantum Dot Gate FETs Using ZnS-ZnMgS Lattice-Matched Gate Insulator on Silicon", *J. Electron. Mater.*, 40, 8, pp. 1749-1756, 2011.

[6] M. Gogna, E. Suarez, P-Y. Chan, F. Al-Amoody, S. Karmakar, and F. Jain, "Nonvolatile Silicon Memory Using GeOx-Cladded Ge QuantumDots Self-Assembled on SiO2 and Lattice-Matched II–VI Tunnel Insulator", *J. Electron. Mater.*, 40, 8, pp. 1769-1774, 2011.

[7] P-Y. Chan, E. Suarez, M. Gogna, B.I. Miller, E.K. Heller, J.E. Ayers, and F.C. Jain, "Indium Gallium Arsenide Quantum Dot Gate Field-Effect Transistor Using II–VI Tunnel Insulators Showing Three-State Behavior", *J. Electron. Mater.*, 41, 10, pp. 2810-2815, 2012.

[8] M. Lingalugari, K. Baskar, P-Y. Chan, P. Dufilie, E. Suarez, J. Chandy, E. Heller, and F.C. Jain, "Novel Multistate Quantum Dot Gate FETs Using $SiO_2$ and Lattice-Matched ZnS-ZnMgS-ZnS as Gate Insulators", *J. Electron. Mater.*, DOI: 10.1007/s11664-013-2696-7, August 2013.

[9] C. Shin, M. H. Cho, Y. Tsukamoto, B-Y. Nguyen, B. Nikolić, T.-J. King Liu, "SRAM yield enhancement with thin-BOX FD-SOI", *Proc. IEEE SOI Conference*, Oct. 5-8, 2009.

[10] F. Jain and F. Papadimitrakopoulos, Patent # 7,368,370, 2008.

[11] M. Lingalugari, P-Y. Chan, P. Dufilie, E. Suarez, P. Mirdha, J. Chandy, E. Heller, and F. Jain, "Multi-State Quantum Dot Gate SOI FETs Using ZnS-ZnMgS-ZnS Lattice Matched Gate Insulators", *Proc. of II-VI Workshop*, 2012.

[12] P. Gogna, M. Lingalugari, J. Chandy, F.C. Jain, E. Heller, and E. Hasaneen, "Efficient Multi-bit SRAMs using Spatial Wavefunction Switched (SWS)-FETs", *Lester Eastman Conference on High Performance Devices (LEC), IEEE Conference Publication,* 2012.

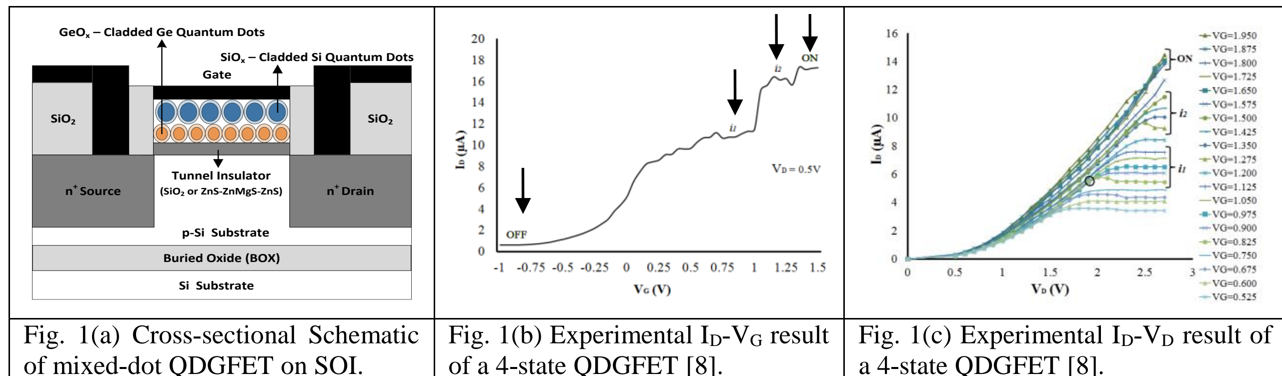


Fig. 1(a) Cross-sectional Schematic of mixed-dot QDGFET on SOI.

Fig. 1(b) Experimental $I_D$-$V_G$ result of a 4-state QDGFET [8].

Fig. 1(c) Experimental $I_D$-$V_D$ result of a 4-state QDGFET [8].

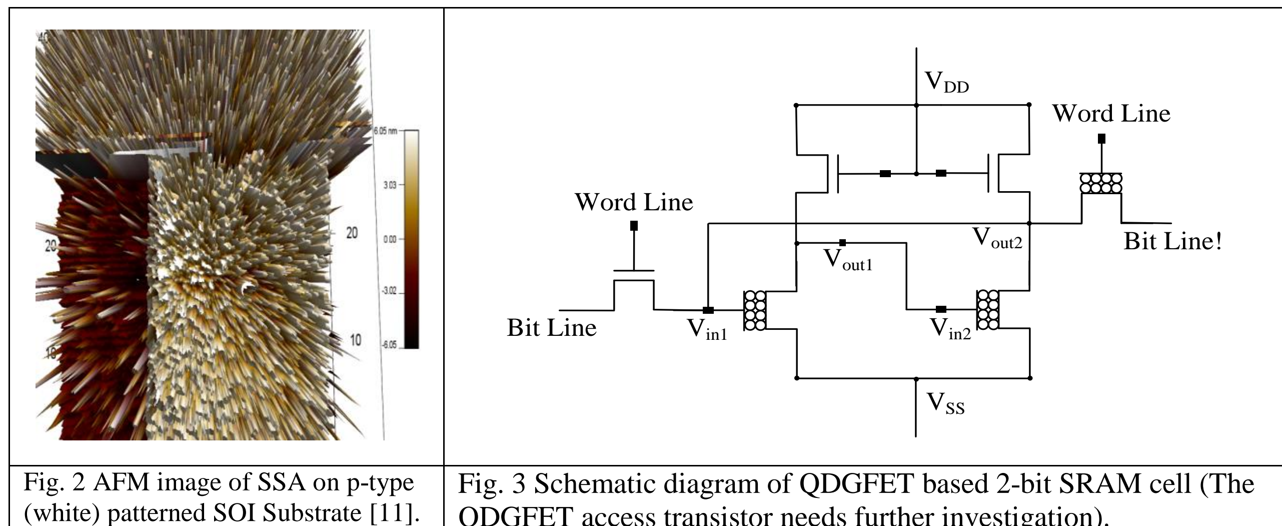


Fig. 2 AFM image of SSA on p-type (white) patterned SOI Substrate [11].

Fig. 3 Schematic diagram of QDGFET based 2-bit SRAM cell (The QDGFET access transistor needs further investigation).