Student Paper

A study on 1T Capacitor-less Tunnel FET DRAM Exploiting Ungated Body

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In this work we report experimental results on capacitorless Tunnel FET (TFET) DRAM cell implemented as a double-gate (DG) fully-depleted Silicon-On-Insulator (FD-SOI) device. The device has an asymmetric design, with a partial overlap of the top gate (L_G) and with a total overlap of the back gate over the channel region (L_G+L_{IN}), which creates the necessary condition to store holes injected from the source-to-body junction in an electrically induced potential well near the drain. The potential well is created by biasing the back gate (V_{BG}) in accumulation while the front gate (V_{FG}) is in depletion and/or inversion. In contrast with the SOI Z-RAM® there is no need of impact ionization to create/inject the hole charge in the device body, the holes being injected by the forward-bias *p+i* junction, which is expected to significantly improve the device reliability. The device principle is scalable in the sub-100nm gate length.

TFETs have been recently proposed [1,2] as steep slope switches able to reduce the voltage operation of logic circuits below 0.2V with reduced leakage current and improved switching energy efficiency. While high-performance Tunnel FETs exploit InAs-Si heterostructures on nanowires [3], the all-Si Tunnel FET family appears primarily to have a very high I_{ON}/I_{OFF} and the lowest I_{OFF} [4] yet fail to achieve the requirements of I_{ON}. In this paper, we show that all-Si DG Tunnel FET can serve for building a new class of devices: the capacitorless TFET DRAM, where the very low I_{OFF} is offering low refresh rate and the zero-capacitor structure very high potential for scalability. Fig. 1 depicts a cross section of the fabricated device. The fabrication of the TFET devices was performed on a SOI substrate with 145nm BOX and 20nm active Si layer using a MESA process [5]. The gate stack was composed of 6nm SiO_2/10nm TiN/50nm Poly Si. The key feature of the one transistor (1T) capacitorless TFET DRAM cell is the possibility to create a potential well that is used to store holes injected from the source-to-body junction when the back gate is in accumulation, V_{BG}<0. TCAD simulations in Fig. 2, 3(a,b) show the hole density and potential profile respectively. This suggests the build-up of a hole pocket in the electrically induced potential well at V_{BG} = -10V (Fig. 3b). It is worth noting that the accumulation in holes of the back gate is also observed in a tunnel FET with the front-gate totally overlapped over the channel, however there *is no potential well* (Fig. 3a) and the carriers are quasi-instantaneously removed from the body. The effect of the back gate on the Tunnel FET front characteristics (threshold voltage shift due to the body potential control and/or charging by the accumulated holes) is clearly seen in Fig. 4; which also demonstrate a good Tunnel FET characteristic with ultra-low I_{OFF} (~10^{-13}A for L_G=500nm, W=10µm) and high I_{ON}/I_{OFF} (~10^5). In the TFET with partially overlapped front-gate and when specific biases ensure the creation of a hole pocket in a potential well, a hysteresis loop is obtained when sweeping back and forth the back gate (Fig. 5). We propose to exploit this effect in order to program the DRAM '1' and '0' levels as summarized in Table 2. The timing diagrams of READ and WRITE operations are shown in Fig. 6. The READ operation is performed with the most negative back gate bias. Depending on the stored state, a clear difference in READ (source) current levels (ΔI_S) is observed (Fig. 7). ΔI_S is more prominent for devices with longer L_{IN}. This experiment demonstrates the importance of the charge storage in the hole pocket outside the front gate overlap, controlled by V_{BG}. Fig. 8 shows a relaxation time in the order of few milliseconds, after the back gate bias is turned off, fulfilling retention requirements of DRAM. The addressing scheme is shown in Fig. 9, pointing out the need for 4-terminal control.

In summary we have demonstrated a scalable 1T capacitorless DRAM cell based on DG Tunnel FET with retention times in the order of 100's of microseconds to few milliseconds, at room temperatures in devices with channel length varying from 400nm to 1µm.

References

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[3] K. E. Moselund et al., IEEE Elect. Dev. Letters, vol. 33, pp. 1453, 2012.
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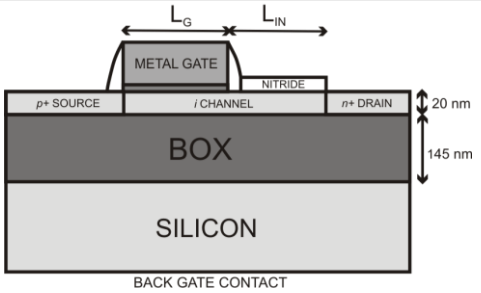

Figure 1: SEM image showing the fabricated 1T Double-Gate Tunnel FET DRAM cell with the top gate overlapped on the channel region L_G and intrinsic region L_{IN} outside the top gate. Inset shows the top view.

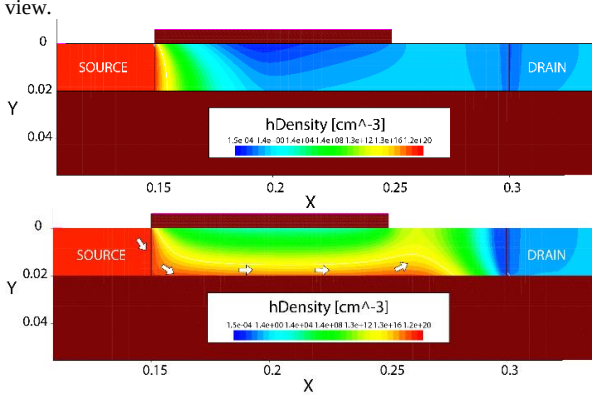

Figure 2: Simulated hole density at WRITE= "0" and at WRITE = "1" for L_G=100nm, L_{IN}=50nm, V_G=5V, V_D=1V, V_{BG}=0V (top) and V_{BG}=-10V (bottom), respectively. A hole pocket accumulation is observed near the drain, at negative back gate bias. The arrows show the injection of holes from the p+ TFET source.

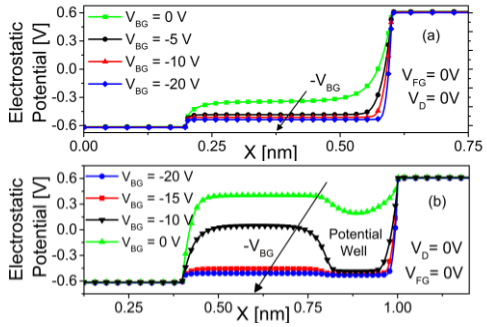

Figure 3: Simulated potential profile at 1nm from BOX with respect to back gate potential for a TFET at V_{BG}=-10V (a) with the front gate overlapped over the whole channel L_G= 400nm, L_{IN}=0nm. No potential well is formed here (b) with underlapped drain, showing the creation of a potential well with L_G=400nm, L_{IN}=200nm..

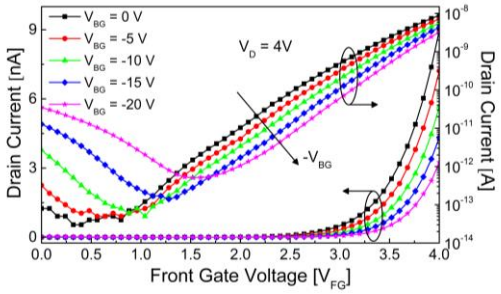

Figure 4: Measured transfer characteristics, I_D-V_{FG} with back gate potential as a parameter, for L_G=400nm, L_{IN}=200nm. This TFET architecture shows significant charge retention and is used as capacitorless DRAM.

Table 2: Programming conditions for indicated operations WRITE '1' and READ of capacitorless 1T -TFET DRAM with L_G=400nm, L_{IN}=200nm. The ERASE also corresponds to WRITE '0'.

State	V_D (V)	V_{FG} (V)	V_{BG} (V)	V_S (V)
WRITE	0	0	-10	0
ERASE	0	0	+10	0
READ	4	4	-10	0

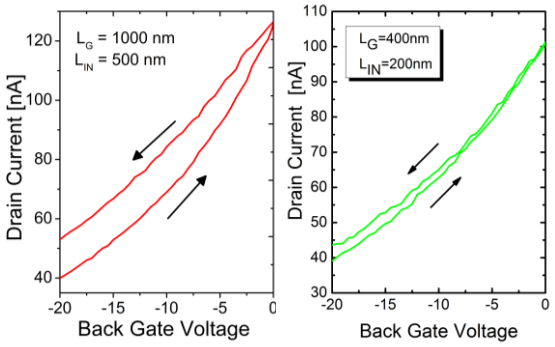

Figure 5: Measured drain current with respect to back gate voltage at fixed front gate and drain voltages, V_G=5V, V_D=4V. A history effect (open hysteresis loop) is observed more prominently in the TFET device with L_{IN}=500nm.

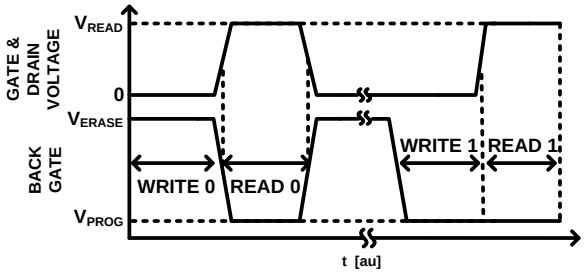

Figure 6: Timing diagram for operations described in Table 1.

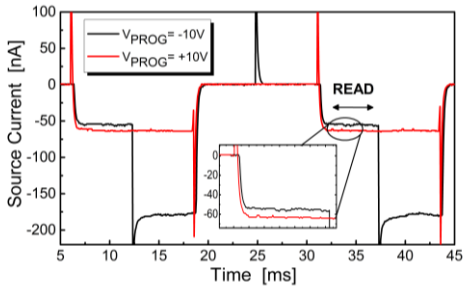

Figure 7: Consecutive READ and WRITE operations for both states. The difference in READ current for states '1' and '0' is 5nA, as highlighted, a memory effect is observed. Programming voltages are: V_{BG}=±10V for TFET with L_G=400nm, L_{IN}=200nm.

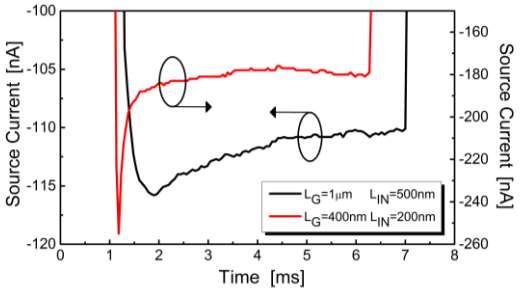

Figure 8: Different relaxation times in the millisecond range are recorded when the back gate is biased at V_{GB}=-10V (after writing 1), depending on the length of the L_{IN} region. The TFET with L_{IN}=500nm shows the longer discharge time while it is negligible in devices with L_{IN}=200nm.

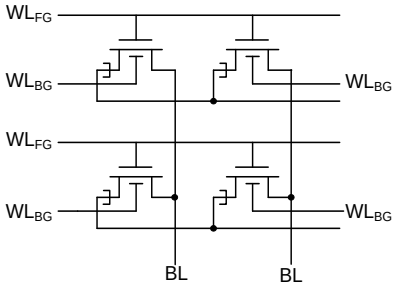

Figure 9: The 1T TFET DRAM cell addressing scheme is based on the use of the both front (WL_{FG}) and back gate (WL_{BG}).