Student Paper

Improvement on a Low Power Neural Amplifier

Samuel A. Gallegos, Hasina Huq

Electrical Engineering Department., The University of Texas-Pan American, *USA, sagallegos1@broncs.utpa.edu*

This work presents an improvement on a Low Power Neural Amplifier described in [1]. The neural amplifier in [1] has a supply voltage of 2.8V, a total current of 2.7µA, for a total dissipated power of 7.56µW and a gain of 40 dB, fabricated in AMI's 0.5-µm CMOS process. The improved neural amplifier presented in this work has a supply voltage of 1.8V, a total current of 59.4nA, for a total dissipated power of 107nW and a gain of 35dB, fabricated in TSMC 25 process.

This type of amplifier is intended to be used in biomedical devices which collect biosignals (Neural in this case) with high fidelity and low power consumption. The purpose of this work is to lower the power consumption of such devices. This is because biophysical signals are typically weak (in the range of a few µV to mV), and these devices are mostly battery-operated. Low power consumption, therefore, is required to reduce battery size, extend operating hours and minimize heat dissipation.

A simplified schematic of the amplifier is showed in Figure 1. Simulations results are show in Figure 3 and Table 1.

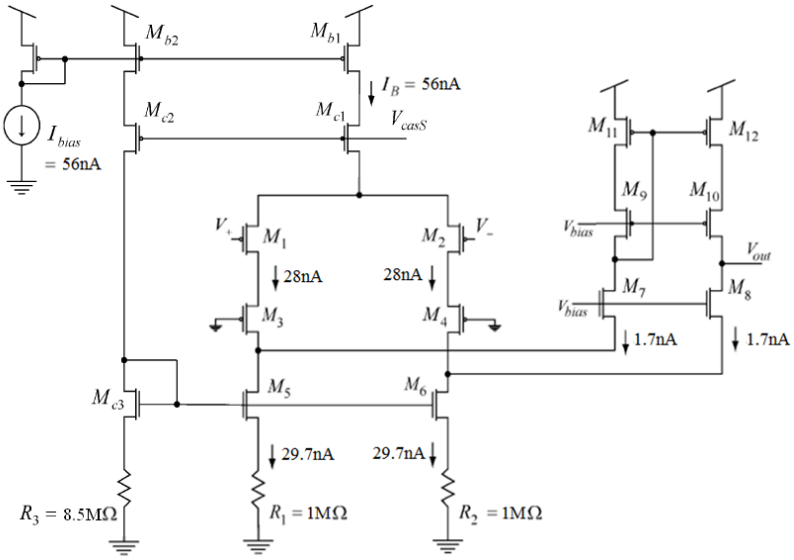

Figure 1. Low Power (107nW) Neural Amplifier [1]

The proposed amplifier is intended for Electroencephalogram (EEG) applications in which, as shown in Figure 2, the biopotential signals vary in magnitude from 1µV to 100µV and in frequency from 1-100Hz.

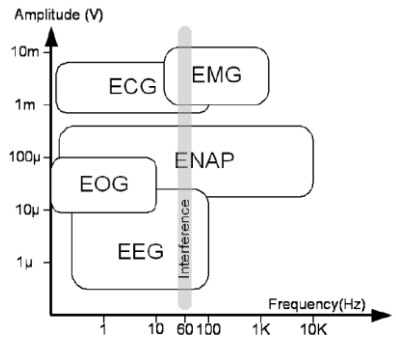

Figure 2. Frequency and amplitude ranges of different biopotential signals [2]

The amplifier is being simulated with a sinusoidal input 10μV in magnitude and with a frequency of 12Hz as shown in the simulation results in Figure 3.

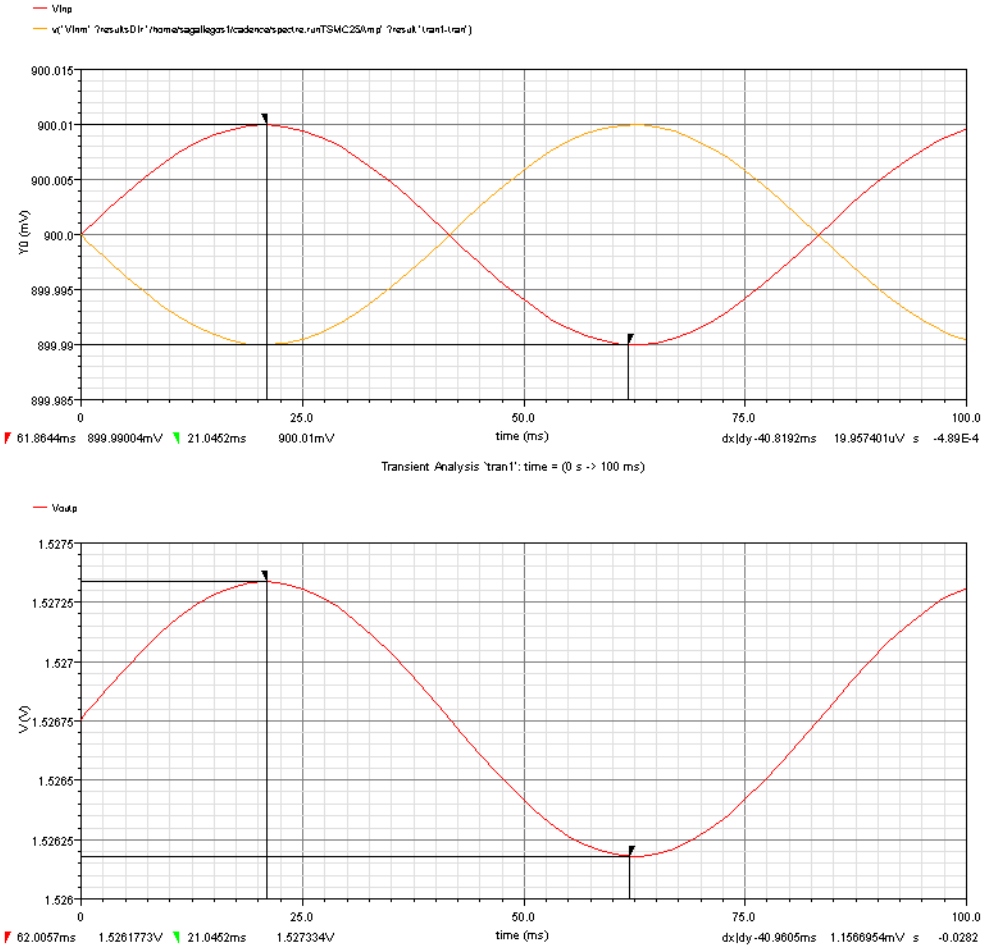

Figure 3. Simulation results: Vout(1.156mV pk-pk) vs Vin(20μV pk-pk) = 35dB Gain

Power Supply Voltage:	1.8V
Total Current Drawn:	59.4nA (from simulation)
Total Power Dissipated:	107nW (from simulation)
Gain:	35dB

Table 1. Parameter simulation results

The amplifier is to be followed by a filter to eliminate interference signals and it is to be fully implemented and fabricated in TSMC 25 process. There are not many results at this point other than simulations; however, the proposed amplifier shows a very significant improvement on the power consumption of the circuit in [1], which as mentioned before benefits greatly the battery powered devices for which this type of amplifier is used.

This work is yet to be completed; it is in the process of simulating the layout before fabricating it and testing the integrated circuit. Physical results and testing using a subject's brain waves are yet to be completed and are all part of future work.

References

[1] Wattanapanitch, W.; Fee, M.; Sarpeshkar, R., "An Energy-Efficient Micropower Neural Recording Amplifier," Biomedical Circuits and Systems, IEEE Transactions on , vol.1, no.2, pp.136,147, June 2007.

[2] Jungsuk Kim; Pedrotti, K.; , "A Low-Power Self-Biased Neural Amplifier for Implantable EEG Recording System ICs," *Engineering in Medicine and Biology Society (EMBC), 2010 Annual International Conference of the IEEE* , vol., no., pp.1573-1576, Aug. 31 2010-Sept. 4 2010.