Low-loss Perforated-Channel HFET

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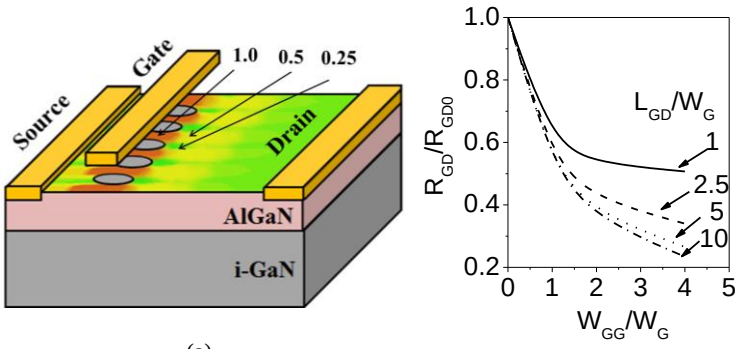
The on-resistance - gate capacitance product, $R_{ON}C_G$, is an important figure of merit of FET switch characterizing the overall power losses [1, 2]. Decreasing R_{ON} by shortening gate-drain spacing decreases the maximum voltage that the power device can operate at and thus typically is not feasible. Reducing R_{ON} by increasing the total device width leads to a larger gate capacitance C_G, which, in turn, leads to higher switching loss. The same $R_{ON}C_G$ figure merit relates to the efficiency of microwave power amplifiers, especially those operating in class E, F and other switching modes [3].

We demonstrate a simple and robust perforated channel (PC) HFET design that reduces the on-resistance without increasing the total gate capacitance. The reduction of R_{ON} is achieved by using the current spreading effect in gate-drain and gate-source regions. Fig. 1(a) shows the schematic of this novel patent pending design for AlGaN/GaN HFET. The portions of the channel under the gate are removed by etching or by any other appropriate technique leaving the channel material in the access regions intact. As a result, the gate - channel capacitance decreases. The source and especially the drain side access resistances are significantly smaller than those for the conventional devices with the same C_G and continuous channel. As a result, the total device $R_{ON}C_G$ product is smaller as well. Known solutions like Heterodimensional HFETs [4, 5] FinFET, tri-gate or multi-mesa FETs also use the channel profiling under the gate [6, 7, 8]. However, the channel profiling in these devices is only feasible using nano-scale islands formed in the channel. In contrast, our design is simple and robust; it produces a significant on-resistance reduction using conventional optical lithography process and can be easily implemented in power FET and IC fabrication.



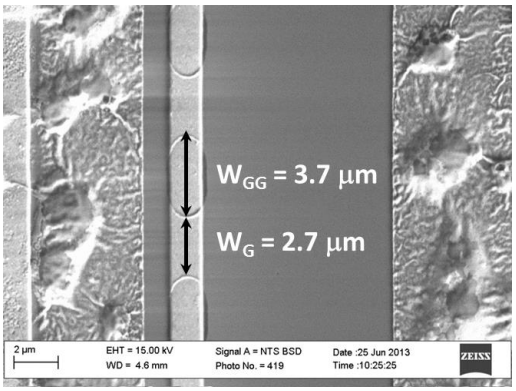
(a) (b)

Fig. 1. Schematic structure and current density pattern in the simulated AlGaN/GaN based PC-HFET. Circles indicate the areas where is channel material is removed. Numbers show normalized channel current density in the points indicated by the arrowheads.

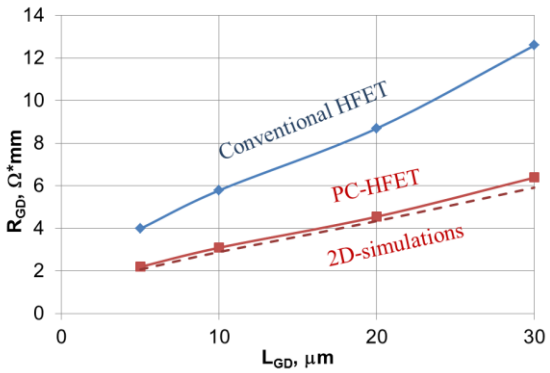
2D simulations of PC-HFET have been performed using Synopsys Sentaurus Device simulator. The HFETs had the channel sheet resistance R_{SH} = 300 Ohm/sq, gate length L_G = 1 μm; the source-gate distance L_{SG} = 1 μm, the gate island width W_G = 2 μm, the spacing between islands W_{GG} = 1 – 10 μm and the gate – drain distance L_{GD} = 1 – 10 μm varied in the simulations. The color pattern in Fig. 1(a) shows simulated normalized current density in the PC-HFET channel with W_G = 1 μm, W_{GG} = 3 μm and L_{GD} = 5 μm at the drain bias below the knee voltage. As shown by the numbers with arrows, the current density in the G-D spacing within only 1 μm off the gate edge reduces almost twice, which indicates a strong current spreading effect in the G-D region. Fig. 1(b) shows simulated PC-HFET G – D region resistance normalized to that of the conventional HFET with the same channel width (i.e. same C_G). As seen, at W_{GG}/W_G = 3 - 4, three-four fold R_{GD} reduction is achievable without increasing the HFET capacitance C_G.

Experimental PC-HFETs have been fabricated on epi-structure consisting of 2 μm thick GaN buffer and 20 nm thick $Al_{0.3}Ga_{0.7}N$ barrier grown on sapphire using Migration Enhanced MOCVD (MEMOCVD®) technique. Inductively coupled plasma etching was used to define mesa pattern and

channel perforation with island width W_G = 2.7 μm and spacing W_{GG} = 3.7 μm (Fig.2 (a)). The island/spacing ratio was in close agreement with the data extracted from C-V of the devices with and without perforation. The holes were then planarized with PCVD SiO_2 film. Ti/Al/Ni/Au metal stack was used to form the ohmic contacts. The Ni/Au gate was deposited by e-beam evaporation and precisely aligned with the perforation openings. The gate length was L_G= 1.5 μm; total (islands plus spacings) gate width was 300 μm. Gate - source spacing was 1.2 μm and gate - drain spacing was varied from 5 to 30 μm. The HFETs were passivated with PECVD deposited SiN_x.



(a)



(b)

Fig. 2. (a): SEM-image of the PC-HFET and (b): experimental (points) and simulated (dashed line) R_{GD} - L_{GD} dependencies for conventional HFET and PC-HFET.

Fig. 2(b) shows experimental gate – drain resistances for conventional and PC- HFETs fabricated on the same substrate. The resistance is normalized to the channel width, i.e. both conventional and PC-HFETs presented in Fig. 2(b) have the same capacitance C_G. Dashed line shows the same dependence from 2D simulations. As seen, PC-HFET shows slower R_{GD} increase with L_{GD} and around two times lower R_{GD} value as compared to conventional HFET. These results confirm the feasibility and great potential of perforated channel design for power HFET applications.

References

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