Student Paper

Improvement of the Memory Properties for Structures with Multi Charge-trapping Layers $HfO_2/Ta_2O_5/HfO_2$ Annealed at Different Temperatures

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As the process technology developing into 20 nm technology-node, charge-trapping memories are developed to replace the traditional floating-gate devices with nonconductive materials as the charge-trapping layer [1, 2]. Among them, the SONOS devices use discontinuous defects in Si_3N_4 layer as charge traps to store the charge carriers. However, the dielectric constant of Si_3N_4 is not high enough to keep up with the process scaling down; and when the layer scales to below 4 nm, its charge-trapping rate reduces greatly [3]. Recently, it is suggested that high-*k* oxides can be used for nonvolatile memories due to their deep-energy charge traps and high dielectric constants, thereby reducing the operation voltage greatly with a large memory window and good retention properties [4, 5, 6]. This paper uses $HfO_2/Ta_2O_5/HfO_2$ (HTH) multi layers as the charge-trapping layers for the first time and investigates the effect of annealing temperature on electrical characteristics of the HTH structures.

The structures were fabricated following the process shown in Fig. 1(a). They were annealed at different temperatures in N_2 ambient for 1 min, including 600 ℃ and 800 ℃. Fig. 1(b) displays the formed structure, with 5 nm/5 nm/2 nm/5 nm/15 nm for the stacked layers of $SiO_2/HfO_2/Ta_2O_5/HfO_2/Al_2O_3$ respectively. The capacitors were analyzed by Agilent B1500A semiconductor characterization system.

Fig. 1(c) is a transmission electron microscopy (TEM) image of the HTH structure annealed at 800 ℃, which shows clear interfaces between different layers. According to the different crystallization temperatures of HfO_2 and Ta_2O_5 layers, 800 ℃ and 600 ℃ only induce different crystalline degree of Ta_2O_5. Fig. 2 presents the energy band of this multi layers structure. Three charge-trapping layers form a gradually deepened potential well. The C-V (1 MHz) hysteresis of the capacitors shown in Fig. 3 indicates that the memory window at ± 15 V sweep voltages increases when Ta_2O_5 is totally crystalline (annealed at 800 ℃). Specifically, it reaches 5 V.

In Fig. 4(a), the flat-band voltage (V_{FB}) shift increases with the applied positive gate voltage. For the structure with totally crystalline Ta_2O_5, the V_{FB} shift during program is larger and saturates at 11 V, gaining a bigger program window. This is because higher temperature annealing treatment induces bigger crystalline grains, which provide more traps for a large memory window, and improve the charge trapping rate as well. Fig. 4(b) shows the effect of annealing temperature on the erase characteristics. When applying a negative gate voltage, the electrons in capacitors annealed at 800 ℃ are easier to tunnel out of the trapping layers due to bigger crystalline grains, and thus a larger erase window is achieved.

Fig. 5 is the retention properties of the capacitors under room temperature. The charge loss speeds for them differ slightly. The gradually deepened potential well and the Al_2O_3 blocking layer annealed at higher temperature contribute to improve device retention [7]. Therefore, annealing treatment at 800 ℃ improves the erase properties of devices without retention deterioration.

In summary, memory characteristics of multi trapping layers $HfO_2/Ta_2O_5/HfO_2$ were investigated. The test results demonstrate that compared to the devices annealed at 600 ℃, both of the program and erase properties improve greatly with only little difference of retention for the structures with Ta_2O_5 crystallized at 800 ℃. Moreover, the capacitors annealed at 800 ℃ exhibit a much larger memory window of 5 V, which have the potential for the future MLC applications.

References

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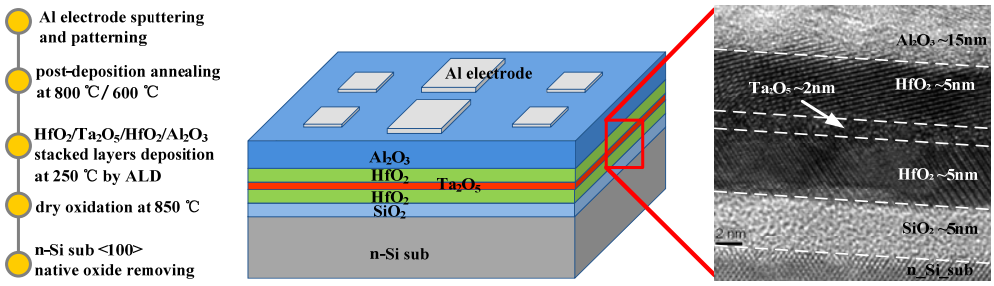


(a) (b) (c)

Fig. 1 (a) Process flow of the structures, (b) Schematic of the capacitors containing multi charge-trapping layers, and (c) TEM image of the structure annealed at 800 ℃.

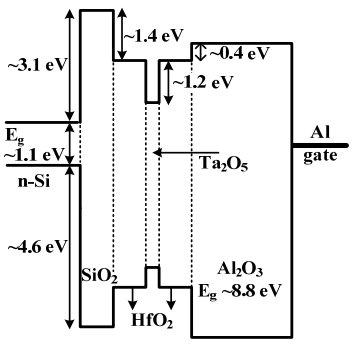
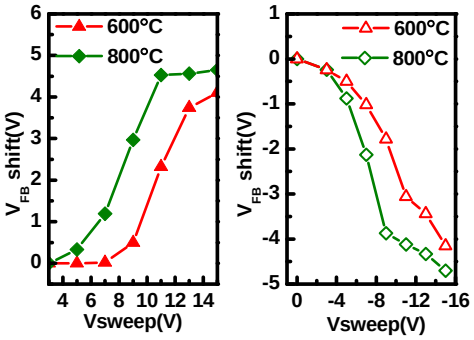


Fig. 2 Schematic energy band diagram of the structures.



(a) (b)

Fig.4 (a) Program properties, and (b) erase characteristics for both capacitors.

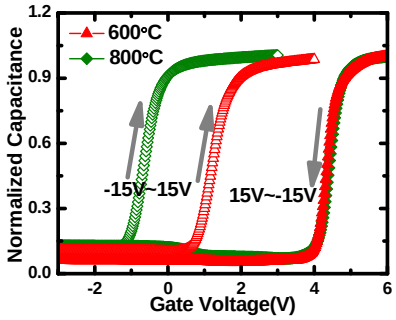


Fig.3 C-V curves of the memory structures. The measurement frequency was 1 MHz.

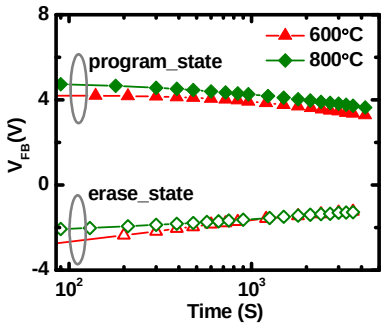


Fig.5 Retention features comparison of the capacitors annealed at 600 ℃ and 800 ℃.