Large Variation of Tunnel-FETs in Comparison with MOSFETs Caused by Sensitivity to Fluctuation of Gate Stack Parameters

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Tunnel-FET (TFET) is a unique device of which current flow is controlled by the band-to-band tunneling (BTBT) at the source junction [1]. It is different from MOSFETs that operate by the control of thermal emission current through the channel. The operation mechanism of TFETs has a potential to reduce the sub-threshold swing to less than 60 mV/decade that is the theoretical limit of MOSFETs at room temperature. Steep sub-threshold swings contribute to the reduction of operation voltage of FETs, and low operation voltages are advantageous for the reduction of power consumption in integrated circuits. TFETs are thus expected for ultra low-power VLSIs in future.

Variation of electrical characteristics among many FETs is a critical issue because it degrades the performance of VLSIs. Thus it is important to observe and understand the variation behaviors of TFETs. In this work, we compared the variation behavior of TFETs and MOSFETs fabricated on an SOI substrate, and studied the origins of variations in combination with simulation.

TFETs and MOSFETs were fabricated on an SOI substrate using a gate-first process flow (**Fig. 1**). The gate stack structures, lithography, dry etching, and the thermal budget in the annealing processes are identical for TFETs and MOSFETs. The ion implantation conditions for the source region of TFETs and the source and drain regions of MOSFETs are the same. The drain region of TFETs is offset from the gate edge by a tilted angle implantation in order to suppress the ambipolar current flow in the operation of TFETs. In this way, p-type TFETs and n-type MOSFETs were fabricated at the same time.

Electrical characteristics of 50 devices of n-MOSFETs and p-TFETs with the same channel sizes (L=500 nm, W=1 um) are shown in **Fig. 2**. They were measured at 243 K in order to suppress the trap assisted tunneling that is known as an origin of variation in TFETs [2, 3]. The results show well-organized performances, however, variations are also observable in both devices.

Influences of gate stack parameters, the work function (WF) of gate electrode and the equivalent oxide thickness (EOT) of gate dielectric film, on the performances of MOSFETs and TFETs are studied by HyENEXSS simulator, which equips non-local BTBT module [4, 5]. The process flow, channel sizes, and measurement conditions for the simulation are identical with the experiment. The results are shown in **Fig. 3**. They reproduced the experimental results sufficiently. It is found that WF and EOT affects on MOSFET and TFET performances in different styles.

The variations of n-MOSFETs and p-TFETs are plotted in **Fig. 4**, together with the trends of variations obtained by the simulation. The off-currents of n-MOSFETs show variation of 2 orders, while the variation of on-currents is unremarkable. The simulation suggests that this trend of n-MOSFET is originated from the sensitivity to the change of WF. It is roughly evaluated that the changes of WF and EOT of the gate stack in this experiment are within 100 meV and 0.2 nm, respectively. In case of p-TFET, on the other hand, both on- and off-currents varies in the experiment (Fig. 4(b)). It is helpful that the variation of off-currents is smaller than MOSFET. However, the large variation of on-currents is a serious problem for the performance of circuits. The simulation demonstrates that TFET is much sensitive to the change of EOT than MOSFET. Thus in order to stabilize the performance of TFETs, gate stack parameters, especially the EOT, must be controlled precisely more than the requirement of MOSFETs.

Acknowledgements

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References

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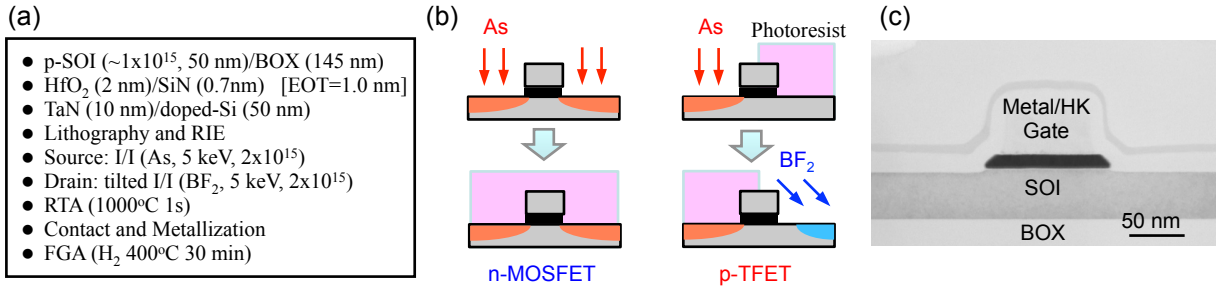

Fig. 1 (a) Process flow of p-TFET. (b) Schematic of ion implantation process for n-MOSFET and p-TFET. (c) Cross sectional TEM image of p-TFET (L_G 100 nm).

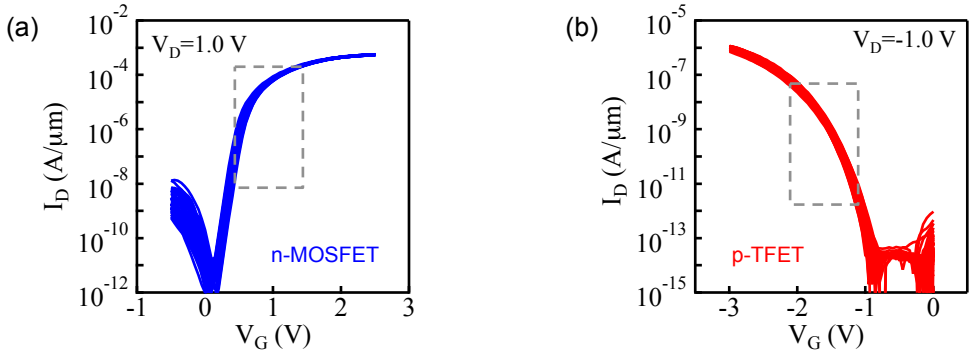

Fig. 2 EXPERIMENT: I_D-V_G characteristics of 50 devices of (a) n-MOSFETs (L/W=500 nm/1 um) and (b) p-TFETs (L/W=500 nm/1 um) measured at 243 K. ON-OFF plots in Fig. 4 were analyzed in the frame region.

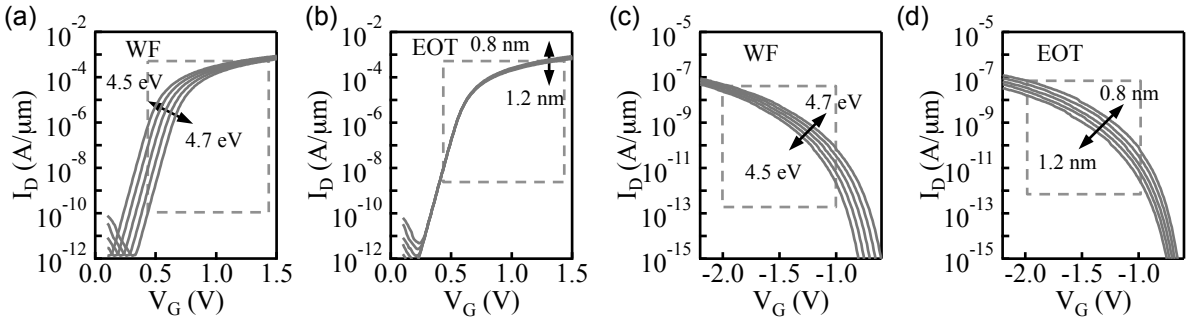

Fig. 3 SIMULATION: Influence of device parameters on I_D-V_G characteristics at 243 K condition. (a) Work function and (b) EOT dependences of n-MOSFETs. (c) Work function and (d) EOT dependences of p-TFETs.

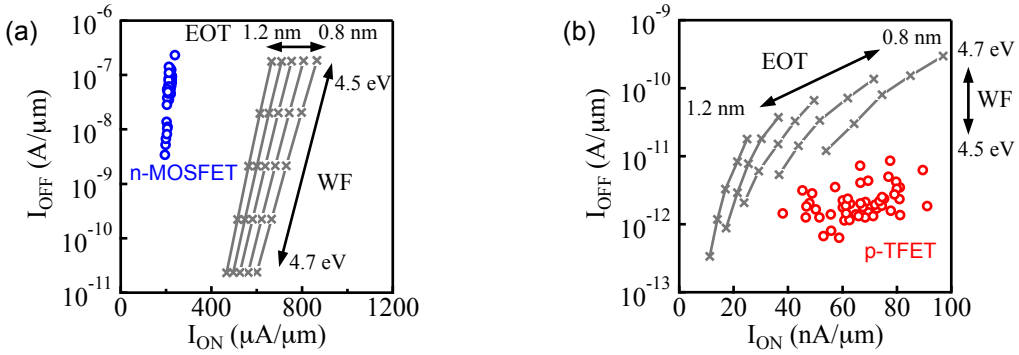

Fig. 4 ON-OFF plots of experimental results of (a) n-MOSFETs and (b) p-TFETs, with the simulation.