Linearity Performance Investigation of high-k Spacer based Junctionless Nanowire Transistor (JLNWT) for RFIC Design

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To meet the modern technological requirements according to the market needs, the device dimensions of the conventional MOSFET are decreasing continuously. The continuous miniaturization of MOSFET at nano scaled regime increases shorts channel effects (SCEs) as well as the fabrication complexity. Due to very high doping requirement and high thermal conditions, the fabrications of the ultra sharp source/drain junctions in nano-scaled MOSFET become more complex. Hence recently a new device, called junctionless transistor [1] has been proposed to alleviate the aforementioned problems. The junctionless nanowire transistors (JLNWT) are uniformly heavily doped throughout the source, channel and drain region and there is no formation of junctions thereby eliminating the problem of the diffusion of the impurities. Although JLNWT shows superior immunity against SCEs and can be scaled to lower channel lengths compared to inversion mode (IM) transistor, but still SCEs are not negligible for such devices. Recent research work focuses that higher ON-state current, minimum OFF- state current and reduced fringing field effects can be achieved by using JLNWT with gate spacer design [2]. Apart from higher performance, device linearity is a crucial parameter for designing the radio frequency integrated circuits (RFIC). Linearity ensures that intermodulation and higher order harmonics are minimal at the output. Intermodulation Distortion (IMD) due to non-linearity, generate unwanted signal with different frequencies. These unwanted (noise) signals may interfere, change or even corrupt the desired output components. So there is need to estimate the linearity distortion analysis for JLNWT with dual k spacer. A transistor-level linearization is more appropriate for power amplifiers in portable systems, which requires an analysis of the linearity behavior at the device level.

So in the present work, linearity distortion analysis of high-k spacer based JLNWT has been carried out. A comprehensive comparative analysis has been presented between JLNWT with spacer and without spacer in terms of Figure of Merit (FOMs) matrices: I_{dsub}, VIP3, IIP3, IMD3 and higher order transconductance coefficient g_{m3}. Figure-1 shows the cross-sectional view of high-k spacer based JLNWT. Here cylindrical gate all around geometry has been taken in consideration due to higher gate controllability and better short channel effects (SCEs) immunity. In this paper 20 nm spacer width and 2 nm gate length is taken. Figure-2 shows the plot between subthreshold current and gate voltage. It is evident from the figure that drain-off current is reduced with high-k spacer. Figure -3 shows the higher order transconductance coefficient g_{m3}. For high linear system, higher order transconductance coefficient should be as minimal as possible. In fig. 3, minimum g_{m3} is analysed with high-k spacer. So the spacer based device shows less linearity than the conventional type. VIP3 represent the extrapolated gate voltage amplitudes at which the third order harmonics, becomes equal to fundamental tone in the device drain current. To achieve high linearity and reliability, these should be as high as possible. Figure 4 shows the higher value of VIP3 in the case of JLNWT with spacer with respect to without spacer. At the second kink point, VIP3 is much higher in case of spacer based device therefore device shows higher linearity. In general, with increase the gate bias, IIP3 increases to the maximum value. Peak of the IIP3 graph, determines the DC bias point for optimum device operation. IMD3 originates from the nonlinearity exhibited by the transistor static characteristics, which causes degeneracy of signals in a wireless communication system. Hence, it is desired to reduce the third- order harmonics for minimizing the signal distortion. From the figure 5 and 6, it is observed that intermodulation distortion can be suppressed by using spacer. Finally the conclusion is that junctionless transistor with high-k spacer improve the device SCEs immunity and also significantly enhances the device linearity. So this device can be used in high linear applications.

References

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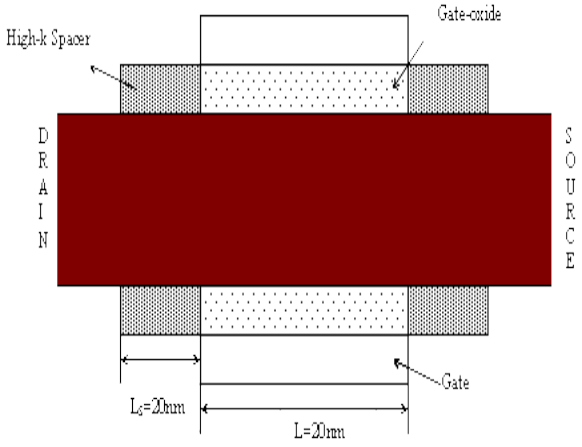
[2] R.A. Baruah, P.P. Paily, "Impact of high-k spacer on device performance of a junctionless transistor" *J. Comput. Electron.*, vol. 12, pp. 14-19,2013.



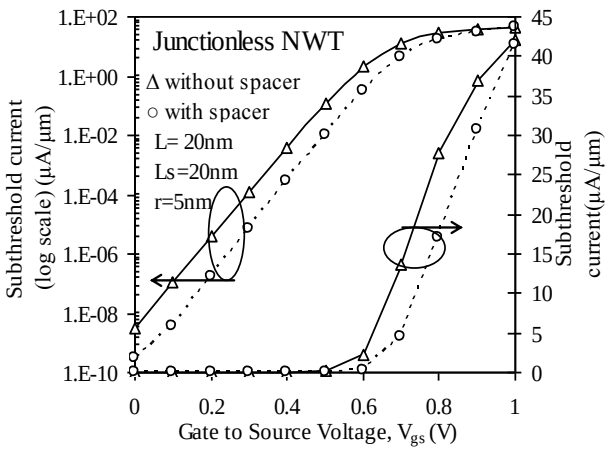
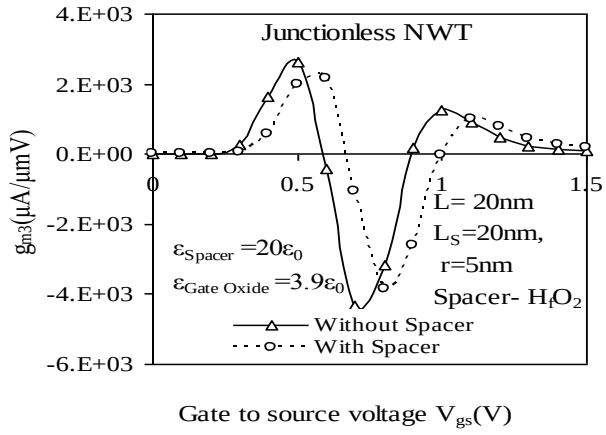


Figure-1 shows the cross-sectional view of high-k spacer based Cylindrical Junctionless nanowire transistor (JLNWT). Fig.-2 shows the normalized subthreshold current verses applied gate voltages for JLNWT with and without high-k spacer.



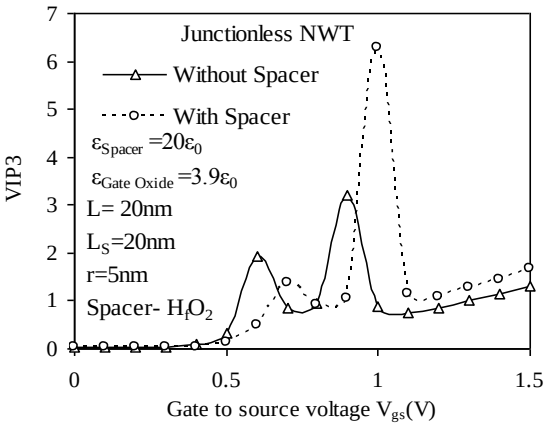
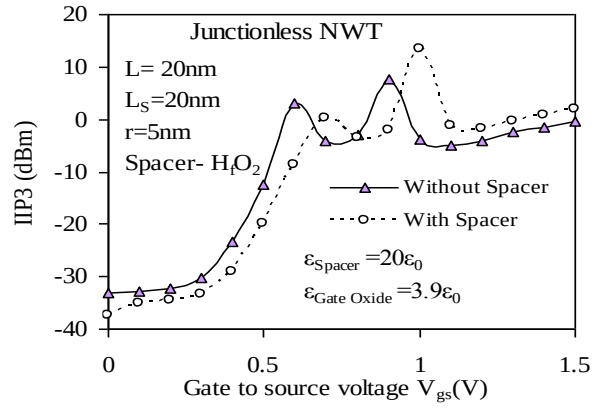


Fig.-3 and fig.-4 show the g_{m3} and VIP3 variations as a function of applied gate bias for junctionless nanowire transistor with and without high-k spacer.



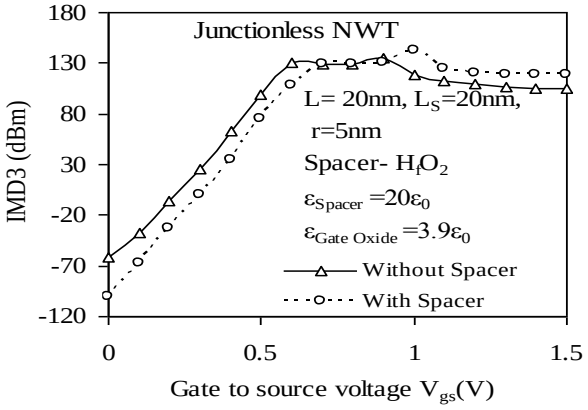


Fig.5. and 6, Variations of IIP3, IMD3 as a function of applied gate bias for JLNWT with and without high-k spacer