Student Paper

The Threshold Voltage Variation on Etch angle of Channel-hole in Vertical NAND Flash memories

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Three dimensional NAND flash memories have been investigated in diverse structures as an alternative to floating gate (FG) NAND flash memories [1]. Since the vertical channel of 3D NAND flash memories allows the ultra-high bit density and low bit cost, it has been considered as the future technology but faced with the reliability issues caused by structural problems. One of the main issues is the etch angle during channel-hole process and it causes the wide V_{th} distribution. In this paper, the effect of etch angle on the threshold voltage of TCAT flash memory was investigated.

Fig. 1 shows the cross sectional image of TCAT flash memory cell simulated by Sentaurus of Synopsys and the concept image of the cell string [2]. The length of each stacked layer is 50 nm and the tunneling oxide-nitride-blocking oxide thickness of each cell is 3 nm, 6 nm and 11 nm, respectively. The radius of each cell is determined by the etch angle of vertical channel hole. As shown in Table. 1, though the target radius of vertical channel hole at the top is set to 40 nm, the radius at the bottom is different according to etch angle. Since each cell has a different radius due to etch angle, it results in the V_{th} in the same bit line. Fig. 2. (a) shows the V_{th} of each cell at the initial state according to etch angles (0.1°, 0.4°, and 0.7°). At lower stack-level cells, the initial V_{th} becomes lower because the inversion in the channel area of the cell with smaller radius occurs at lower gate voltage. At higher etch angle, the distribution of initial V_{th} becomes larger since the difference of radius between cells increases. Fig. 2. (b), (c) and (d) show the V_{th} shift of each cell after program operation in incremental step pulse programming schemes according to etch angles (0.1°, 0.4°, and 0.7°). The target V_{th} and increasing pulse step is 3 V and 0.3 V, respectively. Since larger electric field is applied to the cell having smaller radius, the V_{th} at lower stack-level cells becomes larger. As etch angle of vertical channel-hole becomes higher, since the radius of each cell at the same position becomes smaller, the overall amplitude of V_{th} increases. The overall dispersion of V_{th} also increases as the difference between the radius of each cell becomes larger. The variation of radius in the same bit line induced by etch angle also has an effect on the number of program pulse in ISPP schemes. Fig. 3. (b) shows the average number of program pulse allowing the V_{th} of each cell to reach the target voltage. At 0.1° of etch angle, since the radius variation of each cell in the same bit line is small, all the cells can reach the target voltage by four-times pulses. However, at 0.4° of etch angle, G1 and G2 cells need only three-times pulses to reach the target voltage whereas other cells need one more pulse. The difference of number of pulse causes the difference of degradation between cells and affects the variation of V_{th} in other bit line since all bit lines share the word line as shown in Fig. 3. (a). Fig. 3. (c) shows the distribution of V_{th} programmed from fresh state in inhibit bit line according to the same etch angles as that in program bit line. As etch angle increases, the distribution of V_{th} by program disturbance becomes wide due to the different number of disturbed pulse applied to the cells in inhibit bit line.

In this paper, we investigated the threshold voltage variation by etch angle of channel-hole in vertical NAND Flash memories. At lower stack-level cells, the initial V_{th} decreases whereas the V_{th} increases after program operation due to larger electric field applied to the cells with smaller radius. As the etch angle increases, the increasing variation of radius at each cell causes the dispersion of V_{th} to be increased and affects the number of program pulse applied to each cells to reach the target voltage.

Acknowledgements

This work was supported by Samsung Electronics and Inter-university Semiconductor Research Center (ISRC).

References

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[2] J. Jang et al., "Vertical cell array using TCAT (Terabit Cell Array Transistor) technology for ultra high density NAND flash memory," *VLSI Symp. Tech. Dig.*, pp. 192–193, 2008.

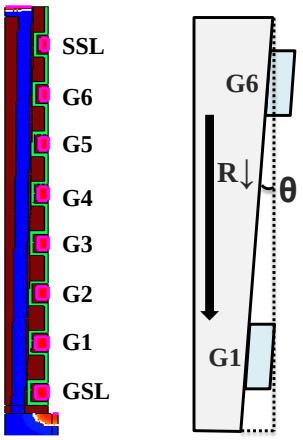

Fig. 1 The cross sectional image and concept image of etch angle in TCAT bit line

Angle(°)	Cell radius at top(nm)	Cell radius at bottom (nm)
0	40	40.000
0.1	40	38.604
0.2	40	37.207
0.3	40	35.811
0.4	40	34.415
0.5	40	33.018
0.6	40	31.622
0.7	40	30.225

Table. 1 The radius at the top and bottom according to etch angle of channel-hole

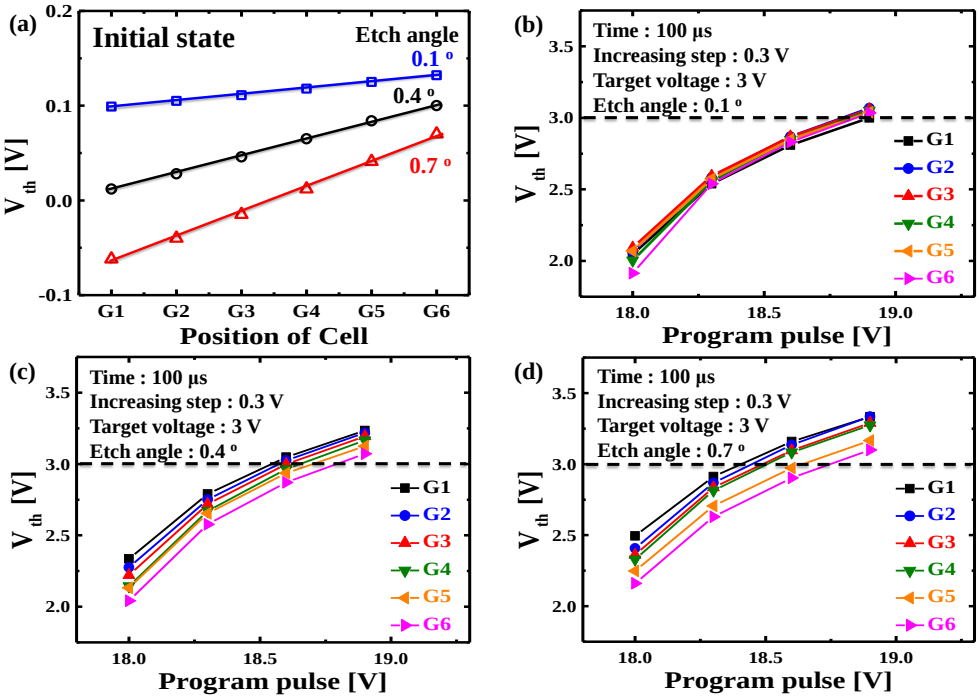

Fig. 2 (a) The V_{th} of each cell at the initial state according to etch angles (0.1°, 0.4°, and 0.7°). (b), (c), and (d) show the V_{th} shift of each cell after program operation in ISPP schemes at each etch angle. The overall dispersion of V_{th} increases at higher etch angle

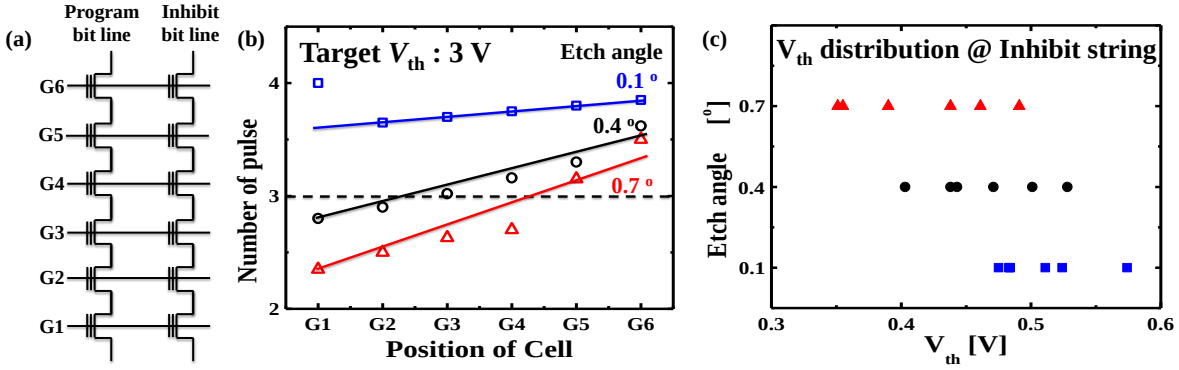

Fig. 3 (a) The schematic of Vertical NAND Flash memory array. (b) shows the average number of program pulse allowing the V_{th} of each cell to reach the target voltage. (c) shows the distribution of V_{th} by program disturbance in inhibit bit line