**Student Paper**

# Analysis of Temperature Dependence and the Apparent Activation Energy ($E_a$) on PV state of Sub 20-nm NAND Flash Memory

Kyunghwan Lee[a], Duckseoung Kang[a], Seongjun Seo[a], Dong Hua Li[b], and Hyungcheol Shin[a]

[a]*Inter-university Semiconductor Research Center (ISRC) and School of Electrical Engineering and Computer Science, Seoul National University, San 56-1, Sillim-dong, Gwanak-gu, Seoul 151-742, Republic of Korea*
*Tel.: +82-2-880-7279, Fax: +82-2-882-4658, E-mail address:viking84@naver.com*
[b]*Product Quality Assurance Team, Memory Division, Samsung Electronics, Korea.*

In order to meet the market demands for memory devices, NAND Flash memory is aggressively scaled down for high-performance and high-density applications. However, the scaling makes them more prone to reliability problems [1]. The retention characteristics of NAND Flash memory are highly complicated and difficult to analyze since there are various failure mechanisms such as detrapping mechanism, TAT mechanism, interface trap recovery mechanism, and so on [2], [3]. In this paper, we analyzed the temperature dependence of retention characteristics and the apparent activation energy ($E_a$) on PV state of the world smallest NAND Flash memory (1X-generation).

Fig. 1 shows the total charge loss of 5K-cycled sub 20-nm NAND Flash memory with baking time up to 1008 hrs at various baking temperature (40ºC, 55ºC, 70ºC, 85ºC, 100ºC, and 125ºC). All the measured data were extracted at lower probability level (P = 0.01) of the $V_{th}$ cumulative distribution of each PV state [4]. The total charge loss is larger as baking temperature and PV state is higher. Fig. 1(d) shows the coefficient of $\Delta V_{th}$ variation (@ 100 hrs) on various baking temperature (40 ~ 125ºC) at each PV state. The results show that the charge loss at lower PV state has larger $\Delta V_{th}$ variation coefficient (PV1 > PV2 > PV3). Fig. 2 (a) shows the retention time of 5K-cycled NAND Flash memory at various baking temperature at PV3 and PV2. The criterion of $\Delta V_{th}$ is 0.2 V. The retention time at PV3 is shorter than the one at PV2 especially at low baking temperature because the TAT mechanism is dominant at low temperature regime and the number of carrier in FG (the source of TAT mechanism) is larger at higher PV state. Fig. 2 (b) shows the apparent $E_a$ at PV3 and PV2 according to the temperature. The values at PV2 are larger than that at PV3 in all temperature regime. The apparent $E_a$ at PV3 is lower as temperature is lower since dominant mechanism is changed. Fig. 3 shows the schematic of energy band diagram of 5K-cycled NAND Flash memory at PV3 and PV2 state. There are various failure mechanisms in NAND Flash memory such as the detrapping mechanism, the TAT mechanism, and interface trap recovery mechanism. Since each mechanism has different retention characteristics and $E_a$, the charge loss behavior is complex. The $E_a$ of each mechanism is generally reported as the following: (The detrapping mechanism: ~ 1.0 eV, the TAT mechanism: ~ 0.3 eV, and the interface trap recovery mechanism: ~ 0.2 eV) [3]. As the portion of the mechanisms with large $E_a$ is larger, apparent $E_a$ is also larger. Since the lower PV state has less electrons in FG, the source of TAT mechanism is small and the relative source of detrapping mechanism is larger. Therefore, the apparent $E_a$ becomes much larger as shown in Fig. 2(b).

In this paper, we analyzed both the variation coefficient of total charge loss ($\Delta V_{th}$) and apparent $E_a$ on PV state. Since there are various failure mechanisms in NAND Flash memory, the retention characteristic shows highly complicated and abnormal behavior. In case of the portion of the mechanism with large $E_a$ such as detrapping mechanism in the total charge loss ($\Delta V_{th}$) is larger, coefficient of $\Delta V_{th}$ variation on temperature and apparent $E_a$ becomes also larger.

**Acknowledgements**

This work was supported by Samsung Electronics and Inter-university Semiconductor Research Center (ISRC).

**References**

[1] M. Kang, et al., "The Compact Modeling of Channel Potential in Sub-30-nm NAND Flash Cell String," *IEEE Electron Device Letter*, vol. 33, no. 3, pp. 321-323, Mar. 2012.

[2] K. Lee, et al., "Analysis of Failure Mechanisms and Extraction of Activation Energies ($E_a$) in 21-nm NAND Flash Cells," *IEEE Electron Device Letter*, vol. 34, no. 1, pp. 48-50, Jan. 2013.

[3] K. Lee et al., "Activation Energies ($E_a$) of Failure Mechanisms in Advanced NAND Flash Cells for Different Generations and Cycling," *IEEE Trans. Electron Devices*, vol. 60, No. 3, pp. 1099-1107, Mar., 2013.

[4] D. Kang, et al., "Generation Dependence of Retention Characteristics in Extremely Scaled NAND Flash Memory," *IEEE Electron Device Letter*, vol. 34, no. 9, pp. 1139-1141, Sep., 2013.

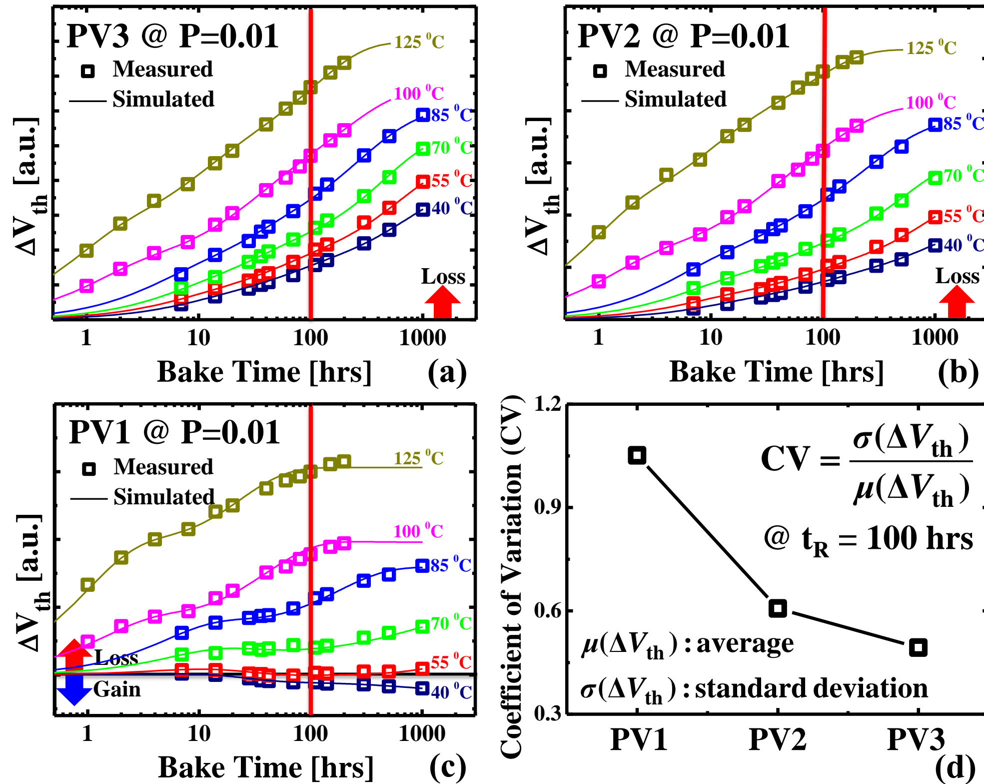


**Fig. 1** The total charge loss at (a) PV3, (b) PV2, and (c) PV1 state of 5K-cycled sub 20-nm NAND Flash memory (@ P=0.01) with baking time up to 1008 hrs at 40ºC, 55ºC, 70ºC, 85ºC, 100ºC, and 125ºC. (d) Variation coefficient of $\Delta V_{th}$ (@ 100 hrs) shows the PV state dependence (PV1 > PV2 > PV3).

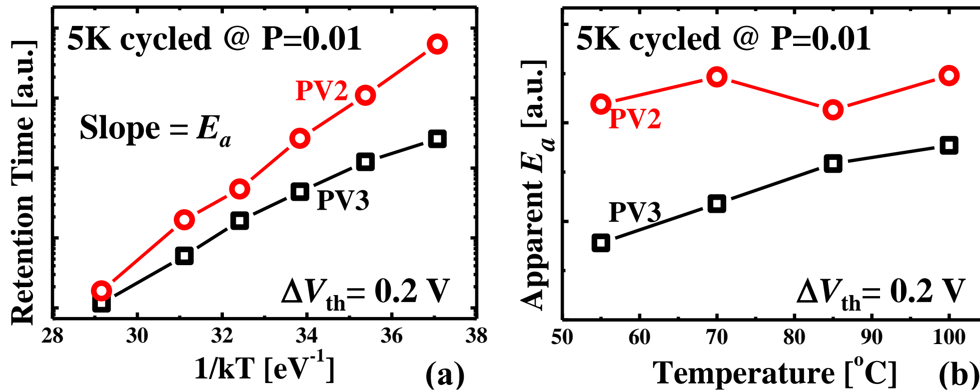


**Fig. 2** (a) Retention time of 5K-cycled NAND Flash memory at various baking temperature (40 ~ 125°C) at PV3 and PV2. The criterion of $\Delta V_{th}$ is 0.2 V. (b) Apparent activation energy ($E_a$) versus temperature [°C]. The $E_a$ at PV2 is larger than the one at PV3 at all temperature regime.

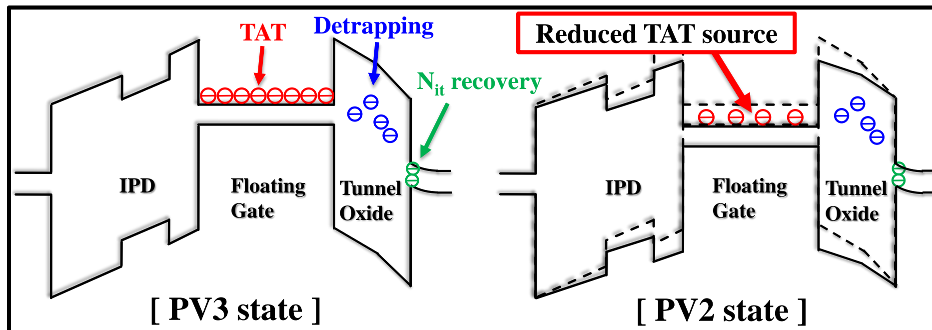


**Fig. 3** Schematic of energy band diagram of 5K-cycled NAND Flash memory at PV3 and PV2 state. The injected number of electrons in FG (the source of TAT mechanism) is much lower and the relative amount of trapped carrier in the tunneling oxide (the source of detrapping mechanism) is larger at PV2 state.