Student Paper

Improved Erasing Speed in Junctionless Flash Memory Device by Bandgap-Engineered Trapping Layer

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Abstract: Operation characteristics of inversion-mode (IM) and junctionless (JL) polycrystalline-Si (poly-Si) flash memory device with HfO_2/Si_3N_4 (HN) bandgap-engineered trapping layer (BETL) are studied and compared in this work. JL device shows faster programming speed than the IM one because of its heavily doped n-channel. Specially, comparable erasing speed of JL device can be achieved by HN BETL due to more effective electron de-trapping. JL device with HN BETL also shows better retention characteristics and keeps a larger window after 10^5 programming/erasing cycles.

Introduction: Recently, poly-Si flash cell technology is becoming attractive due to its potential of three-dimensional (3-D) integration, but its poor DC characteristics are hardly acceptable. Some of the problems can be resolved by JL flash memory device [1], which is generally fabricated on silicon-on-insulator and poly-Si thin-film transistor (TFT) with nanowire (NW) channel. Without additional source/drain (S/D) implantation and activation, the fabrication process of JL device is simplified by simultaneously and heavily doping S/D and channel. The heavily doped channel conducts JL device and can be cut off by being fully depleted. Short channel effect can be minimized by JL device because difficult junction controls such as junction depth and doping concentration are avoided. Furthermore, JL devices with doped n-channel is important for 3-D NAND structure since lower resistance of NAND string can be achieved without complicated S/D implantation. However, the slow erasing speed of JL device is still an issue. Bandgap engineering has been reported for better operation and reliability characteristics. HN BETL has been proposed to improve P/E speeds due to the lower conduction band level and larger trap density of HfO_2 when compared with Si_3N_4 [2]. In this work, HN BETL is applied on both JL and IM flash devices. Characteristics of the two devices are investigated and compared.

Experimental: JL and IM flash memory devices are fabricated on 6-inch Si (100) wafer. Four SiO_2 dummy fins with a height of 100 nm are formed by I-line lithography and reactive ion etching (RIE) process on Si_3N_4 buried layer. An 100-nm thick amorphous-Si is then deposited and transferred into poly-Si by solid-phase crystallization (SPC) process at 600 °C for 24 hours. Samples for JL devices are sent to perform Phosphorous implantation (at 30 keV to a dose of 1×10^{14} cm^{-2}) and activation (900 °C for 30 s). After that, S/D region is defined on two ends of dummy fins for all samples. Eight spacer NW channels are consistently formed with S/D region by precise RIE process control; SiO_2 dummy fins are removed by diluted HF to complete active region. Then, 5-nm SiO_2, 3-nm Si_3N_4, 7-nm HfO_2, 15-nm Al_2O_3 are sequentially grown and deposited as gate dielectrics. TiN is deposited as metal gate. IM devices are sent to perform Phosphorous implantation after gate region formation. All samples are then sent to go through passivation and metallization processes, completed after sintering at 400 °C for 30 min.

Results and Discussion: Fig. 1 shows the transmission electron microscopy (TEM) image of JL device with HN BETL. The width of a NW is about 10 nm, which is narrow enough for NW channels to be effectively controlled by multiple gates. The transfer characteristics of JL and IM devices at $V_{DS} = 0.5$ V are shown in Fig. 2. The subthreshold swing (SS) of JL device is lower because the bulk conduction of JL device is less sensitive to the defective SiO_2/poly-Si interface. The inset shows the transconductance (Gm) versus gate voltage of JL and IM devices at $V_{DS} = 0.5$ V. The higher Gm peak for JL device implies the abundant carriers in the doped channel. Fig. 3(a) shows the programming speeds of JL and IM devices at $V_{GS} = 15$ V. JL device shows faster programming speed, which may be due to its electron-rich channel. More electrons can be injected and captured in trapping layer during programming operation. Fig. 3(b) shows the erasing speeds of JL and IM devices at $V_{GS} = -15$ V with a previous window of 2.4 V. The V_{th} shift refers to devices' program state. With HN BETL, JL device shows comparable erasing speed to that of IM one. It may be due to the more effective electron de-trapping from HN BETL such that the effects of fewer holes are minor. Fig. 4(a) shows the retention characteristics for JL and IM devices with a programmed window of 2 V. The charge loss for JL devices is less under all test conditions, because the JL device is less sensitive to the defects at channel surface and thus the charge leakage is suppressed from

trapping layer. The endurance characteristics of JL and IM devices are shown in Fig. 4(b). The window closure of JL device is less due to its larger initial window for the same P/E conditions. For the case of identical initial window (not shown), the window closure of JL device is also less due to its lower voltage or shorter time for P/E operations.

Conclusions: With HN BETL, JL device shows faster programming speed and even comparable erasing speed, which is rarely seen on JL device with Si_3N_4 trapping layer. The more effective electron de-trapping plays an important role in erasing operation despite the fact that there are fewer holes in n-channel. Good retention and endurance performances in JL device are also demonstrated. Therefore, JL flash memory device with HN BETL is a promising candidate for 3-D memory integration in the future.

References

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[2] Z. H. Ye, K. S. Chang-Liao, C. Y. Tsai, T. T. Tsai, and T. K. Wang, "Enhanced operation in charge-trapping nonvolatile memory device with charge-trapping layer," *IEEE Electron Device Lett.*, vol. 33, no. 10, pp. 1351 –1353, Oct. 2012.
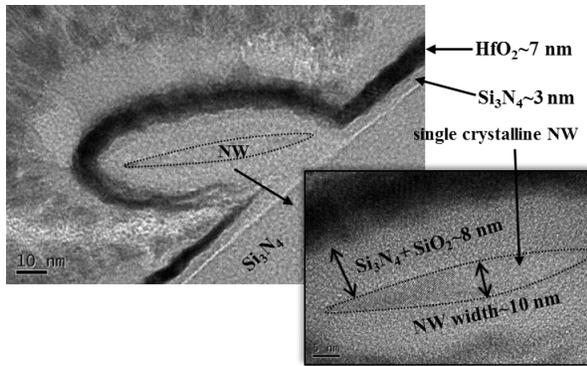
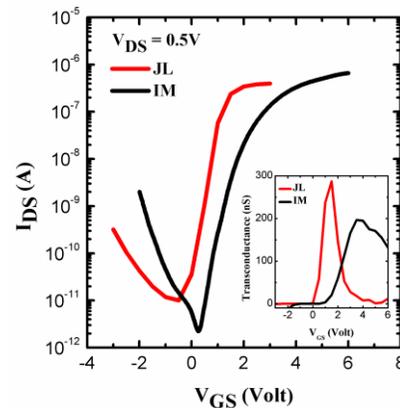Fig. 1 Cross-section TEM image of JL flash device with HN BETL.

Fig. 2 Transfer characteristics of JL and IM devices . A comparison of transconductance versus V_{GS} is also plotted in the inset.
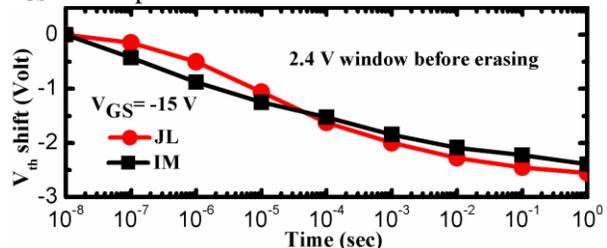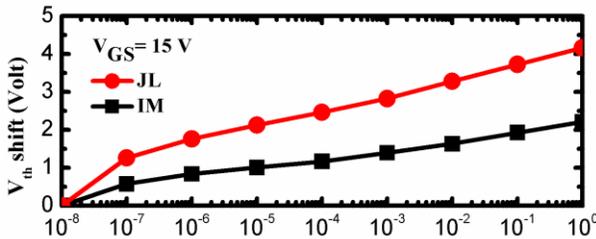

Fig. 3 Memory operations of JL and IM devices. (a) Programming speed at V_{GS} = 15 V. (b) Erasing speed at V_{GS} = -15 V with a previous window of 2.4 V.
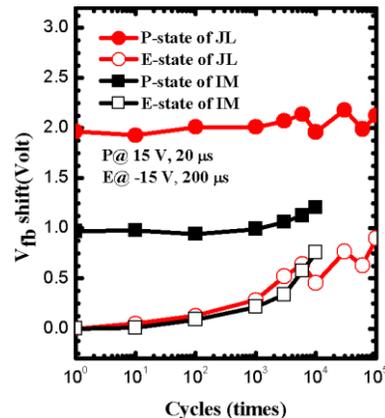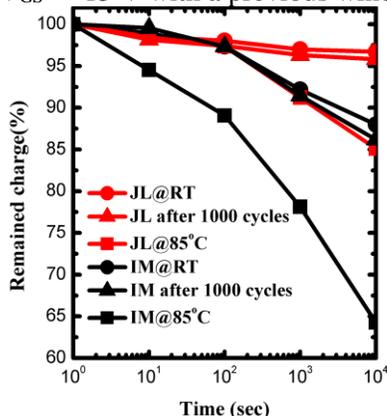

Fig. 4 (a) Retention and (b) endurance characteristics of JL and IM devices.