Student Paper

Multi-Level Storage Capacity and Performance Improvement by Stacked Layers in Metal Oxide RRAM Devices

Fang Yuan[a], Zhigang Zhang[a], Liyang Pan[a] and Jun Xu[a]

[a] *Institute of Microelectronics, Tsinghua University, China, yuanf09@mails.tsinghua.edu.cn*

Many binary metal oxide materials have been discovered for the resistive random access memory (RRAM) applications and exhibit good non-volatile memory performance [1]. In this study, aluminum oxide (AlO_x) and hafnium oxide (HfO_x) were chosen as resistive memory layers because of the CMOS compatibility in film fabrication. After standard RCA clean of Si substrate and thermal evaporation of 100-nm-thick Pt as bottom electrode (BE), 20-nm AlO_x, 20-nm HfO_x, 15nm- HfO_x/5-nm AlO_x, and 15-nm AlO_x/5-nm HfO_x were deposited via atomic layer deposition. 100-nm-thick Ag was deposited as top electrode (TE) and patterned by circular shadow mask with the diameter of 100 μm. The four splits of devices were sequentially numbered 1-4# for simplicity as shown in Fig. 1. All the RRAM devices were measured by an Agilent B1500A semiconductor parameter analyzer by applying DC voltage on TE and grounding BE.

Fig. 2 shows the typical current versus voltage (*I-V*) characteristics of 1-4# splits. All the devices show bipolar resistive switching behaviors with positive bias operations to set and negative bias ones to reset. The set voltage ranges from +0.4V to +0.8V and decreases when AlO_x composition shrinks, which implies that pure AlO_x films need larger voltage than pure HfO_x films to be set to low resistance state (LRS). In addition, for single layer devices (1# and 2#), the reset operation is one sudden drop of current. But for bilayer devices (3# and 4#), it takes several stages for current to drop to reset the device to high resistance state (HRS). In Fig. 3, the increase of maximum reset current and decrease of LRS resistance as a function of the set compliance current of all the 4 splits strongly suggest a filament-based switching, which means positive V_{set} excludes Ag ions/atoms from TE into film to form conductive filaments penetrating the film bulk while negative V_{reset} draws back Ag ions/atoms to rupture the filaments [2].

Specially, 4# split (15-nm AlO_x/5-nm HfO_x) has a multi-level storage capacity achieved by controlling the V_{stop} in reset operations, as shown in Fig. 4(a). When the negative V_{stop} increases, the LRS device can be reset to a more complete extend, leading to a larger high resistance so that the V_{set} required in next switching cycle will increase (Fig. 4(b)) [3]. Fig. 5(a) and (b) shows the retention performance of 4 splits. 1# (AlO_x) fails in LRS due to the lack of electrical field to maintain Ag filaments aligned from TE to BE. 2# (HfO_x) fails in HRS because of the diffusion of Ag in the film, which can easily establish sufficient filaments as each read operations brings more Ag ions/atoms into film bulk. 3# (HfO_x/AlO_x) performs well in both HRS and LRS. 4# (AlO_x/ HfO_x) proves at least five stable resistance states and each resistance level can maintain in retention. For these two bilayer splits, the great performance improvement can be attributed to the inducement of a charge-rich interface between the two stacked layers. The interface behaves as a barrier and offers a relatively steady charge storage region. Thus, the filament cannot easily be changed from its formal status.

Fig. 6 is a schematic diagram of proposed model for 4# stack-layered RRAM devices. The black lines represent conducting filaments and they can be formed/ruptured in three regions: (1) within AlO_x film bulk, (2) within HfO_x film bulk, and (3) at the interface. Therefore, the total resistance of the device can be viewed as a series of three resistances: $R_t = R_{Al,t} + R_{Int,t} + R_{Hf,t}$. Each resistance $R_{*,t}$ is a sum of several paralleled $R_{*,0}$. Since the interface is a charge-rich area, the filaments here are stable and difficult to grow/rupture. When filaments forms/breaks down as a sequence of different V_{stop}, the $R_{*,t}$ will change, so that the total resistance R_t will theoretically have several levels of value. But in order to be identified with a memory window large enough and easily operated, only five levels were picked up in this work.

In conclusion, stacked layers have been proved to significantly improve memory performance in metal oxide RRAM devices. The stacked layers induce an interface, which strengthens the retention properties and expands the multi-level storage capacity. It is a promising candidate for future high-density, low-consumption memory applications.

This work was supported by the State Key Development Program for Basic Research of China (No. 2011CBA00602), and the National Natural Science Foundation of China (No. 20111300789).

References

[1] H.-S. P. Wong, H.-Y. Lee, S. Yu, Y.-S. Chen, Y. Wu, P.-S. Chen, B. Lee, F. T. Chen, and M.-J. Tsai, "Metal–oxide RRAM," *Proc. IEEE*, vol. 100**,** pp. 1951, 2012.

[2] K. Tsunoda, Y. Fukuzumi, J. R. Jameson, Z. Wang, P. B. Griffin, and Y. Nishi, "Bipolar resistive switching in polycrystalline TiO_2 films," *Appl. Phys. Lett.*, vol. 90, pp. 113501, 2007.

[3] H. Y. Lee, P. S. Chen, T. Y. Wu, Y. S. Chen, C. C. Wang, P. J. Tzeng, C. H. Lin, F. Chen, C. H. Lien, and M.-J. Tsai, "Low Power and High Speed Bipolar Switching with A Thin Reactive Ti Buffer Layer in Robust HfO_2 Based RRAM," *IEDM Tech. Dig.*, pp. 1-4, 2008.

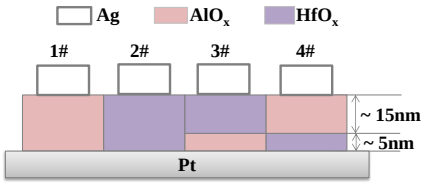

Fig.1 Schematic structure of 1-4# RRAM devices.

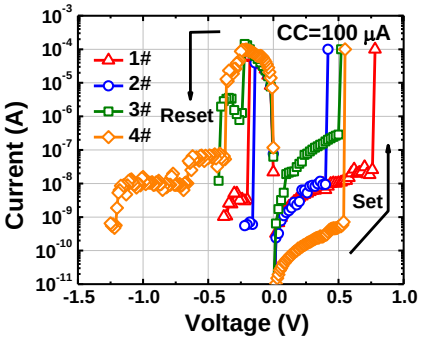

Fig.2 Typical current versus voltage (I-V) curves of 1-4# RRAM devices.

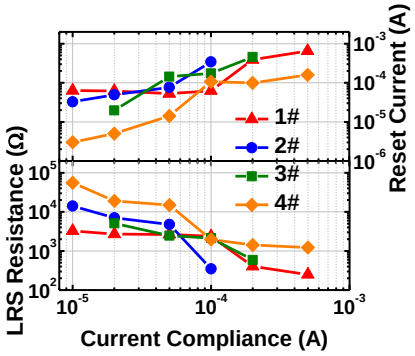

Fig.3 Maximum reset current and LRS resistance as a function of the current compliance.

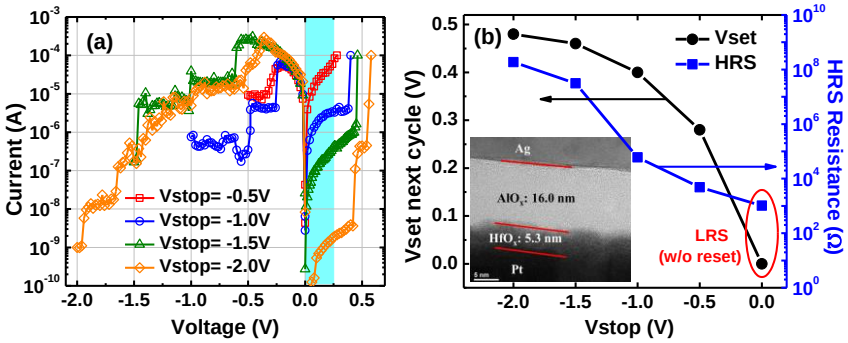

Fig.4 (a) Multi-level storage realization controlled by reset voltage in 4# devices. (b) HRS resistance and set voltage in next DC cycle as a function of reset voltage. The inset is HRTEM image of 4# stacked layers.

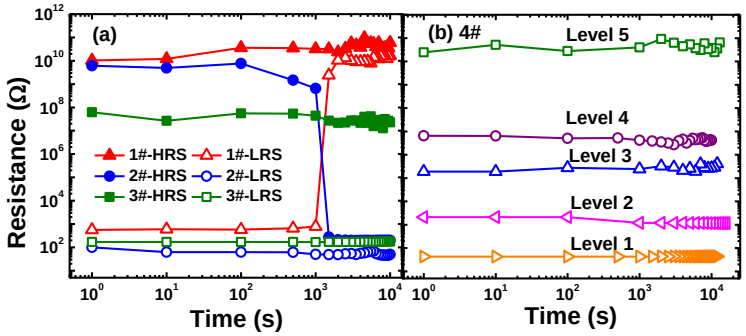

Fig. 5 (a) Retention performance of 1-3# RRAM devices and (b) Multi-level retention performance of 4# RRAM devices.

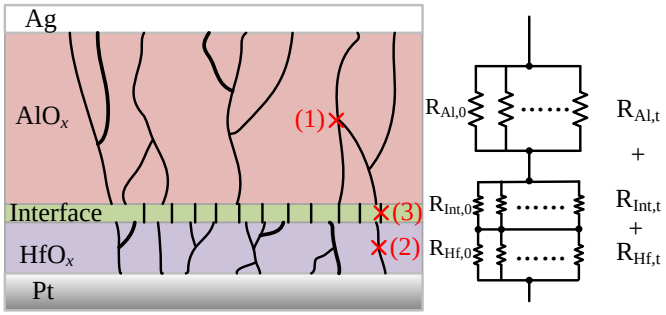

Fig. 6 Schematic of proposed switching model for stack layers in 4# RRAM devices.